KS20937

E-TELEMETRY STATION TEST SET SYSTEM

Scientific-Atlanta, Inc.

New Jersey Division

Specialists in Electronic Instrumentation

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E-TELEMETRY STATION TEST SET SYSTEM

INSTRUCTION MANUAL

MODEL NO.
SERIAL NO.
OWNER
PURCHASE ORDER NO.

This manual is furnished under contract for the SCIENTIFIC-ATLANTA, INC. instrument listed above and contains instructions for the operation and calibration of the instrument for its intended use. The information contained in this manual shall not be either referred outside the owner's facility or used, duplicated, or disclosed in whole or in part for manufacturer or procurement without the written permission of SCIENTIFIC-ATLANTA, INC.

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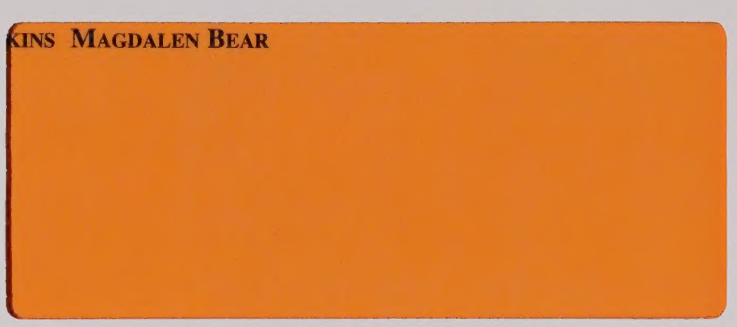
KINS MAGDALEN BEAR

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CLAIM FOR DAMAGE IN SHIPMENT

The instrument should be tested as soon as it is received. If it fails to operate properly, or is damaged in any way, a claim should be filed with the carrier. A full report of the damage should be obtained by the claim agent, and this report should be forwarded to us. We will then advise you of the disposition to be made of the equipment and arrange for repair or replacement. Include model number and serial number when referring to this instrument for any reason.

WARRANTY

Scientific-Atlanta, Inc., New Jersey Division warrants each instrument manufactured by them to be free from defects in material and workmanship. Our liability under this warranty is limited to servicing or adjusting any instrument returned to the factory for that purpose and to replace any defective parts thereof. Electronic tubes and batteries are specifically excluded from any liability. This warranty is effective for one year after delivery to the original purchaser when the instrument is returned, transportation charges prepaid by the original purchaser, and when upon our examination it is disclosed to our satisfaction to be defective. If the fault has been caused by misadjustments, misuse, or abnormal conditions of operation, repairs will be billed at cost. In this case, an estimate will be submitted before the work is started.

Calibration checks of this instrument can easily be made in accordance with the instruction manual. Routine adjustments **should never** be attempted. If, however, the instrument has been damaged and requires recalibration or alignment, explicit calibration procedures as defined in the instruction manual **must** be followed.

If any fault develops, the following steps should be taken:

1. Notify us, giving full details of the difficulty, and include the model number and serial number. On receipt of this information, we will give you service data or shipping instructions.

2. On receipt of shipping instructions, forward the instrument prepaid, to the factory. If requested an estimate of the charges will be made before the work begins provided the instrument is not covered by the warranty.

SHIPPING

The instruments should be packed in their original containers, or in a strong exterior container and surrounded by two inches of shock absorbing material.

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A D D E N D U M

KS-20937 E-Telemetry Station Test Set is manufactured by Quan-Tech to meet KS-20937 specifications as well as a commercial version of the same system. The KS-20937 is electrically equivalent to the 2400 series E-Telemetry Station Test Set referenced in this manual.

Listed below is a part number cross reference for all models included in the E-Telemetry Station Test Set.

KS-20937	Quan-Tech Model	Description
List 1	2474	Basic Test Set
List 2	2476	E1/E2 Manual Alarm Central Plug-In Model A
List 3	2475	E1/E2 Manual Alarm Central Plug-In Model B Remote Call-Up
List 4	2477	General Purpose Plug-In
List 5	8592	E1/E2 Cable
List 6	8593	E2A Cable
List 7	8594	Transit Case
List 8	8597	TCT Test Cable
List 9	A8721	Remote Test Extender
List 10	A8722	Status Scanner Tester
List 11	A8723	Pairer Status Tester
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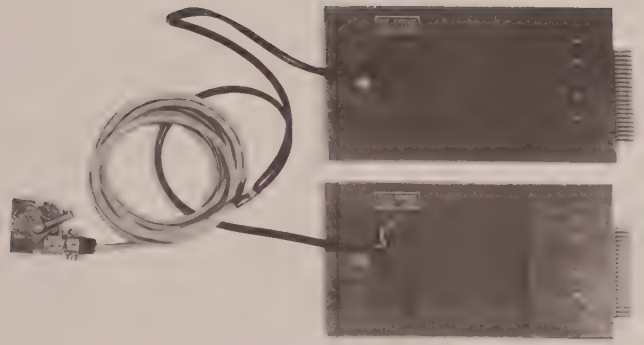
MODEL 2474
BASIC TEST SET

MODEL 2476
E1/E2 MANUAL ALARM
CENTRAL-B

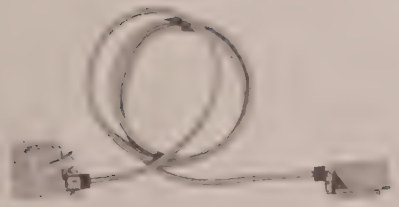
MODEL 2475
E1/E2 MANUAL ALARM
CENTRAL-A

MODEL 2477
GENERAL PURPOSE
PLUG-IN

FIGURE 1-1
E-TELEMETRY STATION TEST SET
AND PLUG-IN UNITS

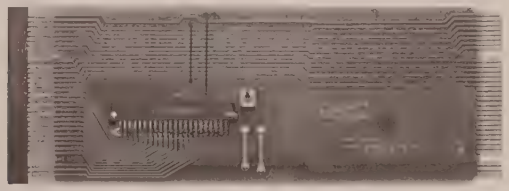


E1/E2 TEST CABLE, 8592

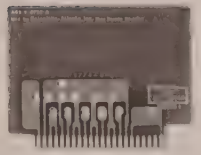


E2A TEST CABLE, 8593

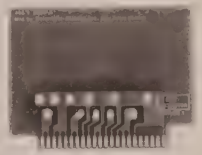
TCT TEST CABLE, 8597



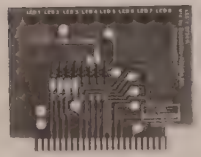
E2A REMOTE EXTENDER, 8721



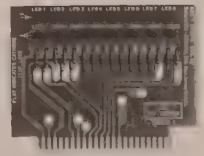
E2A SS TESTER, 8722



E2A PS TESTER, 8723



E2A CI/O TESTER, 8724



E2A CD TESTER, 8725

TRANSPORT CASE

FIGURE 1-2
E-TELEMETRY STATION TEST SET
TRANSPORT CASE
AND TEST CABLES

General Information

1-1. INTENDED USE OF THE STATION TEST SET AND PLUG-INS

1-1a. The E-Telemetry Station Test Set exercises the capabilities of remote and central stations of the E1 and E2 Status Reporting and Control Systems, and the E2A Telemetry System for verification of proper operation or fault location within said equipment. To accomplish this purpose, the Basic Test Set (Model 2474) when equipped with the proper Plug-In Models 2475, 2476, or 2477), will format and transmit serial data to E-Telemetry equipment, receive serial data from the E-Telemetry equipment and display selected received data in parallel. The Remote Call Up (RCU) feature of those E2 remote stations so equipped can be exercised using the proper plug-in.

1-2. PURPOSE AND USE OF THIS MANUAL

1-2a. The purpose of this instruction manual is to provide the user with the necessary information for the proper operation of the Models 2474, 2475, 2476 and 2477. This information includes instructions necessary for minor repairs, routine maintenance and trouble shooting if required.

1-2b. Section 1 of this manual contains all the technical data defining the physical, electrical and performance characteristics of the Basic Test Set (Model 2474) and Plug-In (Model 2475, 2476, or 2477) herein referred to as the **TS/PI** combination or **E-Telemetry Station Test Set.**

1-2c. Section 2 contains all the technical instructions required for the proper operation of the E-Telemetry Station Test Set. However, it is recommended that the user become familiar with the entire manual prior to operating the equipment.

1-2d. Section 3 contains technical discussions of the design technique used in the E-Telemetry Test Set. The reader will find it convenient to refer to block diagrams contained in this section and schematic diagrams contained in Section 7 while reviewing this section. The schematic diagrams are conveniently reproduced on foldout sheets that allow simultaneous visual coverage of schematics and the technical discussion.

1-2e. Section 4 provides instructions for routine care and maintenance and **CAUTIONS** to be observed when performing them.

1-2f. Section 5 is designed to aid the technician as to the proper technique in making minor repairs. This section is necessary because most of the equipment employs COS/MOS I.C.'s which are more susceptible than conventional TTL logic to installation damage.

1-2g. Section 6 contains a systematic approach to trouble shooting including a "Sympton and Probable Cause" chart and applicable waveforms.

1-2h. Section 7 contains the following:
1) Schematic Drawings
2) Component Locations
3) Replaceable Parts List
4) Semiconductor Legend
5) Connector Lug Identification

1-3 DESCRIPTION OF THE EQUIPMENT

1-3a. The Model 2474, Basic Test Set (BTS) and choice of Plug-In (PI) Model 2475, 2476 or 2477 are the components of the E-Telemetry Station Test Set. The BTS is the heart of the system in that it provides all control signals, timing gates, modes of operation and interfacing levels both to the users equipment and to its own PI module. It is the TRANSMIT/RECEIVE CONTROL CENTER.

1-3b. The Model 2476 and 2475 PI's, E1/E2 MANUAL ALARM CENTRALS B and A, respectively, function as semi automatic transmit data programmers. Power and control signals are supplied to them from the BTS. They are semi automatic in that they must be manually set for a desired programmed instruction, but will automatically change the word format of transmitted messages. The Model 2476 differs from the Model 2475 only in the amount of instructions that it contains i.e. 6 as compared to 4 in the 2475.

1-3c. The Model 2477 GENERAL PURPOSE PI is used as a manual transmit data programmer and again does not have a self contained power supply. It must receive this as well as control signals from the BTS to function. The data format is manually set with the 4 rows of toggle switches on its front panel. Each row corresponds

to the data format of a word. The top row is word 1, the second row is word 2 and so on. It has the capability of supplying a 1, 2, 3, 4, or 16 word message to the BTS for transmission. This capability is front panel selectable. In addition to the above, the Model 2477 has a REMOTE CALL UP (RCU) feature which allows the receiving E-Telemetry Station Test Set to receive a 1 word message and answer in acordance with the data content in the first 3 bits of that word.

1-3d. The E1/E2 TEST CABLE, P/N 8592, provides the electrical connection between the Model 2474 and the E1/E2 Station under test. Connection of the Model 2474 to the data facility or telephone network is accomplished using this test cable.

1-3e. The E2A TEST CABLE, P/N 8593, provides the electrical connection between the Model 2474 and the E2A Station under test. Connection of the Model 2474 to the data facility or telephone network is accomplished using the test cable.

1-3f. The TRANSPORT CASE is designed to store the Model 2474, spare plug-in, applicable manuals and associated cables.

1-3g. The E2A TCT TEST CABLE, P/N 8597, provides the electrical connection between the Model 2474 and the E2A Station under test providing a TCT test capability.

1-3h. The REMOTE TEST EXTENDER, P/N 8721, is used as an extender board for E2A remote status and command circuit boards and provides a printed circuit board connector to accommodate P/N 8722, 8723, 8724 and 8725 circuit board testers.

1-3i. The STATUS SCANNER TESTER, P/N 8722, test board provides input signals for E2A remote status scanner circuit boards CP9 and CP35.

1-3j. The PAIRER STATUS SCANNER, P/N 8723, test board provides input signals for E2A remote paired status scanner circuit board CP10.

1-3k. The COMBINED I/O TESTER, P/N 8724, test board provides input signals and output monitor LED's for E2A remote combined input/output circuit boards CP6, CP24 and CP37.

1-3l. The COMMAND DECODER TESTER, P/N 8725, test board provides output monitor LED's for the E2A remote command decoder circuit board CP11.

1-4. PHYSICAL CHARACTERISTICS

1-4a. The E-Telemetry Station Test Set and currently available PLUG-IN UNITS are shown in Figure 1-1. The transport case and test cables are shown in Figure 1-2. The cabinet, panels and other structural members are fabricated from aluminum. The cabinet in which the Basic Test Set (Model 2474) is permanently installed is equipped with two carry handles for easy transportability. The bottom of this cabinet is equipped with feet and a bail for sloping the instrument during bench operation.

1-4b. The Model 2474 and cabinet together weigh approximately 27 lbs. The Models 2477, 2475 and 2476 Plug-In Units weigh approximately 8, 9 and 10 lbs. respectively. The total approximate weight of the Model 2474 and cabinet with a plug-in unit and interconnecting cable is 37 lbs.

1-4c. Overall dimensions of the E-Telemetry Test Set including handles, feet cable and panel protrusions are 15" high x 16-1/2" wide x 14-3/4" deep. The overall dimensions for any individual plug-in unit are 9-9/16" high x 16-1/16" wide x 13-1/4" deep.

1-4d. Transport Case — Overall dimensions of the transport case are 19-1/4" high x 31-3/8" wide x 21-3/4" deep. The transport case weighs approximately 50 lbs. unloaded.

1-5. ELECTRICAL POWER CHARACTERISTICS

1-5a. The instrument is supplied from the factory for 105 to 130 Volt — 55/65 Hertz (Hz) operation. The power requirement is approximately 23 volt-amperes and is fused at the rear with a Bussman Type MDL slo-blo 3/4 ampere fuse.

1-5b. It is recommended that if replacement of the line cord is required, that only a three conductor power cord equivalent to that which was originally supplied on the instrument be used. It should be noted here that the power supply and signal common in this equipment is isolated from chassis ground. For maximum performance of the equipment, however, it is recommended that power to the Test Set be obtained from a proper grounded polarized outlet. This also serves as good safety practice.

1-6 PERFORMANCE SPECIFICATIONS

1-6a. The detailed performance specifications for the E-Telemetry Station Test Set are presented in Table 1-1.

TABLE 1-1. PERFORMANCE SPECIFICATIONS

BIT RATE
Range: Selectable 150, 600 or 1200 Serial Bits/Sec.
Accuracy: ± .01%

MESSAGE SEPARATION
Continuous Mode:
6 Sec, +30%, −15% at 150 B/S
2 Sec, +30%, −10% at 600 B/S
.5 Sec, +30%, −15% at 1200 B/S

WORD SEPARATION
Multi-Word Messages in E1/E2: 6 Bits Minimum
Multi-Word Messages in E2A: 1 Continue Bit Logic "1"

VALID WORD INDICATOR
Illuminated for: 15 Milli Sec Minimum

EXTERNAL RECEIVE ENABLE SENSITIVITY
+Ext. Voltage Transition:
From 0 Volts, +.5 Volts, −0 Volts
To +14 Volts ± 12 Volts
−Ext. Voltage Transition:
From +14 Volts ± 12 Volts
To 0 Volts, +.5 Volts, −0 Volts

E1/E2 INPUT SIGNAL LEVELS
$\overline{TMT}$, $\overline{GR}$: Logic 1 = 0 Volts, +.5, −0 Volts
Logic 0 = +21 Volts ± 5 Volts, at 3 ma (Sink)
TD: Logic 1 = 0 Volts, +.5, −0 Volts
Logic 0 = +6 Volts to +27 Volts at 6 ma (Sink)

E1/E2 OUTPUT SIGNAL LEVELS
RD, TONE: Logic 1 = 0 Volts, +.5, −0 Volts
Logic 0 = +21 Volts ± 5 Volts at 3 ma (Sink)

E2A INPUT SIGNAL LEVELS
RTS, DTR, TDI: Logic 1 = +8 Volts ± 3 Volts
Logic 0 = −8 Volts ± 3 Volts
SD: Logic 1 = −8 Volts ± 3 Volts
Logic 0 = +8 Volts ± 3 Volts

E2A OUTPUT SIGNAL LEVELS
CTS, CD, RIND: Logic 1 = +8 Volts ± 3 Volts
Logic 0 = −8 Volts ± 3 Volts
RD: Logic 1 = −8 Volts ± 3 Volts
Logic 0 = +8 Volts ± 3 Volts

POWER INPUT
Voltage: 105-130 Volts
Frequency: 55-65 Hz.

INTERFACE PROTECTION
All input and output circuitry interfacing directly with either E1/E2 or E2A equipment can withstand the application of ± 30 Vdc or a short to ground indefinitely.

LIST OF ABBREVIATIONS

A GATE B — Buffered A Gate
AR — Alarm Report
B GATE B — Buffered B Gate
C — Capacitor
CD — Carrier Defect
CLK — Clock
CR — Diode
CTS — Clear to Send
DR — Display Report
DTR — Data Terminal Ready
EN — Enable
EXT RCV — External Receive
GR — Group Report
Hz — Hertz
IN — Input
INFO — Information
INSTR — Instruction
KHz — Kilohertz
LED — Light Emitting Diode
MASTER CLOCK B — Buffered Master Clock
PAR — Parallel
PI — Plug In
QR — Quick Reply
R — Resistor
RCU — Remote Call Up
RCV — Receive
RD — Receive Data
RS — Remote Switch
R/T — Receive/Transmit
RTS — Ready to Send
SER — Serial
TD — Transmit Data
TMT — Transmit
TMTL — Transmit Logic
VR — Voltage Regulator
+ EXT — Positive External
− EXT — Negative External

Operation Instructions

2-1. SCOPE OF THIS SECTION

2-1a. The material covered in this section will provide the user with sufficient instructions for the proper operation of the E-Telemetry Station Test Set equipment. However, it is recommended that the more technical material covered in Section 3, Principles of Operation, be reviewed first. A thorough understanding of the design techniques of the equipment will enhance its usefulness.

2-1b. Figures 2-1 through 2-4 are provided in this section as foldouts to illustrate the locations of controls, indicators and connectors on both the front and rear panels of the Model 2474 and each of the Plug-In units. They are designed to be used in conjunction with Tables 2-1 through 2-4 which give a written description of the functions of these controls, indicators and connectors.

2-2. DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS.

2-2a. Table 2-1 and Figure 2-1 together describe and locate the controls, indicators and connectors of the Model 2474 Basic Test Set.

2-2b. Tables 2-2 and 2-3 and Figures 2-2 and 2-3 inclusive describe and locate the controls, indicators and connectors of the Models 2476 and 2475, (E1/E2 Manual Alarm Centrals B and A) respectively.

2-2c. Table 2-4 and Figure 2-4 describe and locate the controls, indicators and connectors of the General Purpose Plug-In (GPPI) — Model 2477.

2-2d. Table 2-5 indicates the function of the connectors associated with the interconnecting cable and various test cables.

2-2e. The Transport Case contains 3 compartments for accommodating one Model 2474 containing a plug-in unit, one spare plug-in, instruction and maintenance manual and test cables.

2-3. PREPARATION FOR USE AFTER SHIPMENT.

2-3a. Inspect the instrument for signs of physical damage. This instrument requires a 3-prong power connection providing a good ground connection. DO NOT operate this instrument without proper grounding.

2-3b. The following cables are available with each E-Telemetry Station Test Set and should be connected as described below:

Interconnecting Cable — 8770
E1/E2 Test Cable — 8592
E2A Test Cable— 8593
E2A TCT Test Cable — 8597

Connect one end of the interconnecting Cable to the Model 2474 rear connector (J1) and the other end to connector (J1) of the Plug-In used. This cable is reversible in that either end may be connected to the BTS or PI. NOTE: All cable ends attached to the E-Telemetry Station Test Set equipment are keyed. They can only be seated properly in one position. Observe this keying before trying to force the cable onto the mating connector. Once seated firmly, lock into place using the locking levers on the cable plug housing. After determining the data system to be used, connect either the E1/E2, E2A or TCT in a similar manner as above to the (J2) connector of the Model 2474. Connect the other end to the STATION UNDER TEST. The equipment is now ready for "turn on" and operation.

2-4 OPERATING PROCEDURE

2-4a. Once power has been applied to the instrument, the MASTER CLEAR pushbutton should be depressed to clear all circuitry in the BTS and PI modules. All front panel controls on the BTS and PI should be set for the type of operation desired and data to be transmitted. Reference to the DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS in this section will aid the operator in preparing the instrument for use. Once all controls are set, depression of the START button will initiate the instrument cycling.

2-4b. DO NOT change the BIT-RATE during transmission as erroneous transmission or reception will result.

2-4c. If it is desired at any time to check the front panel indicators for proper operation, depress INDICATOR TEST button. All lamps should illuminate.

2-4d. "Checkerboard Pattern" - When using the Model 2476 PI with REMOTE CALL UP instruction initiated, one of two checkerboard patterns can be selected for Words 2-16, either pattern A or B. In position A, all even numbered words (2, 4, 6, ... 16) contain logic 1's in even bits (2, 4, 6, ... 16) and logic 0's in odd numbered bits (3, 5, 7, ... 17). Odd numbered words (3, 5, 7, ... 15) contain logic 1's in odd bits (3, 5, 7, ... 17) and logic 0's in even bits (2, 4, 6, ... 16). In position B, the pattern is reversed. Even numbered words contain logic 1's in odd bits and odd numbered words contain logic 1's in even bits.

TABLE 2-1
MODEL 2474
CONTROLS, INDICATORS AND CONNECTORS

SYSTEM rotary switch (S8)	Selects either the E1/E2 or E2A Telemetry System data formats to be received or transmitted.
PARITY rotary switch (S9)	Selects either the A or B parity checking method.
BIT RATE rotary switch (S5)	Selects the data rate-either 150, 600, or 1200 serial bits per second.
TMT lamp (LED 26)	Illuminated during each transmit interval.
DTR lamp (LED 27)	Illuminates upon receiving a logic "1" level signal on the DATA TERMINAL READY (DTR) Line. The Logic "1" level occurs when E2A equipment is ready to transmit or receive.
RCV lamp (LED 28)	Illuminated during each receive interval.
MODE rotary switch (S6)	Selects the following transmit modes: a) ONCE – the programmed message in the plug-in is transmitted one time when the START button is depressed. b) CONT. – the programmed message in the plug-in is transmitted continuously once the START button is depressed with a message separation which is dependent upon the data rate. c) ANSWER – the programmed message in the plug-in is transmitted upon completion of each received message.
MASTER CLEAR push button switch (S2)	Operation of this control button clears all registers and counters and resets all control circuits as well as clearing displays in both the basic test set and plug-in.
START push button switch (S7)	Initiates transmission
E2A CONT lamp (LED 25)	This lamp is illuminated (logic "1") for all words of an E2A MESSAGE except the last word. It is always blanked when the system is E1/E2.
RECEIVE PARITY lamps (LEDS 18-24)	Indicates the state of each parity bit of the 25 bit received word. An illuminated lamp indicates a logic "1".
RECEIVE INFORMATION lamps (LEDS 1-17)	Indicates the state of each information bit of the 25 bit received word. A logic "1" state is indicated by an illuminated lamp.
RCV EN IN binding post (E1)	If external receive enable is desired, the enable trigger is applied to this post.
RCV GRD binding post (E2)	Ground post for above ext. enable trigger.
INDICATOR TEST push button switch (S3)	When this button is held depressed, all indicators on the Model 2474 and Plug In will illuminate.
ENABLE switch (S4)	Selects the following receive enable modes: a) NORMAL – Reception automatically enabled at the beginning of each received message. b) +EXT. – Reception enabled by beginning of next received message after positive logic "0" to "1" transition on RCV EN IN input. c) –EXT. – Reception enabled by beginning of next received message after positive logic "1" to "0" transition on RCV EN IN input.
ERROR WORD lamp (LED 29)	Illuminates upon reception of each invalid word.
VALID WORD lamp (LED 30)	Illuminates upon reception of each valid word.
DISPLAY ERROR WORD toggle switch (S10)	With this switch in the ON position, the **first** word in error will be latched into the display.
DISPLAY WORD SELECT rotary switch (S11)	Selects ALL or 1 of 16 words to be displayed.
RECEIVER CLEAR push button switch (S1)	Clears the word counter, the display error word circuits and the display. **Only** receive circuits are affected.
POWER lamp (LED 1)	Illuminated when AC line power is applied to the instrument.
POWER toggle switch (S12)	Applies AC line power to the instrument when in the ON position.
J2 connector (J2)	Provides a mechanical means of interfacing the E-Telemetry Station Test Set with other E-Telemetry equipment.
J1 connector (J1)	When interconnected with J1 on a Plug-In, supplies D.C. power and control signal levels to the Plug-In and receives outputs from the Plug-In.

TABLE 2-2
MODEL 2476 CONTROLS, INDICATORS AND CONNECTORS

STATION	thumbwheel switch (S8A)	Programs bits 7, 8 and 9 of word 1 in all instructions **except** the QUICK REPLY instruction. (LSB=bit 7).
	thumbwheel switch (S8B)	Programs bits 4, 5 and 6 of word 1 in all instructions **except** the QUICK REPLY instruction. (LSB=bit 4).
REMOTE SWITCH	thumbwheel switch (S6A)	Programs bits 14, 15, 16 and 17 of word 1 of the REMOTE SWITCH instruction **only**. (LSB=bit 17).
	thumbwheel switch (S6B)	Programs bits 2, 3, 4 and 5 of word 2 of the REMOTE SWITCH instruction **only**. (LSB=bit 2).
	thumbwheel switch (S6C)	Programs bits 6, 7, 13 and 14 of word 2 of the REMOTE SWITCH instruction **only**. (LSB=bit 6) and the most significant bit (MSB) is bit 4.
GRP/I/O	thumbwheel switch (S7)	Programs bits 14, 15, 16 and 17 of word 1 of the GROUP REPORT, DISPLAY REPORT and REMOTE CALL UP (RCU) instruction. (LSB=bit 17).
DISPLAY	thumbwheel switch (S5)	Programs bits 13 and 14 of word 2 of the DISPLAY REPORT instruction. (LSB=bit 13).
REMOTE SWITCH	push button switch (S4) and lamp (LED 4)	Interlocked instruction switch which initiates specific instruction data formats. The lamps illuminate upon depression of their respective instruction switch.
DISPLAY REPORT	push button switch (S3) and lamp (LED 3)	
GROUP REPORT	push button switch (S2) and lamp (LED 2)	
ALARM REPORT	push button switch (S1) and lamp (LED 1)	
REMOTE CALL UP	push button switch (S13) and lamp (LED 6)	
QUICK REPLY	push button switch (S12) and lamp (LED 5)	
DI ON/OFF	toggle switch (S11)	Inserts a logic "0" when OFF or a logic "1" when ON in bit 12 of the 1 word QUICK REPLY instruction message ONLY.
TE/NE	toggle switch (S10)	With this switch in the TE position, a logic "1" is inserted in bit 13 of the single word QUICK REPLY instruction message ONLY. In the NE position a logic "0" is inserted.
IMED REPLY ON/OFF	toggle switch (S9)	Places a logic "1" in bit 13 of word 1 of the (RCU) instruction when in the ON position or a "0" in the OFF position.
DATA PATTERN A/B	toggle switch (S14)	Selects either A or B checkerboard patterns to be transmitted in words 2 through 16 of the RCU instruction. See paragraph 2-4d for checkerboard pattern description.
J1	connector (J1)	Permits connection (with use of an interconnecting cable) to J1 of the Basic Test Set Model 2474.

TABLE 2-3
MODEL 2475
CONTROLS, INDICATORS AND CONNECTORS

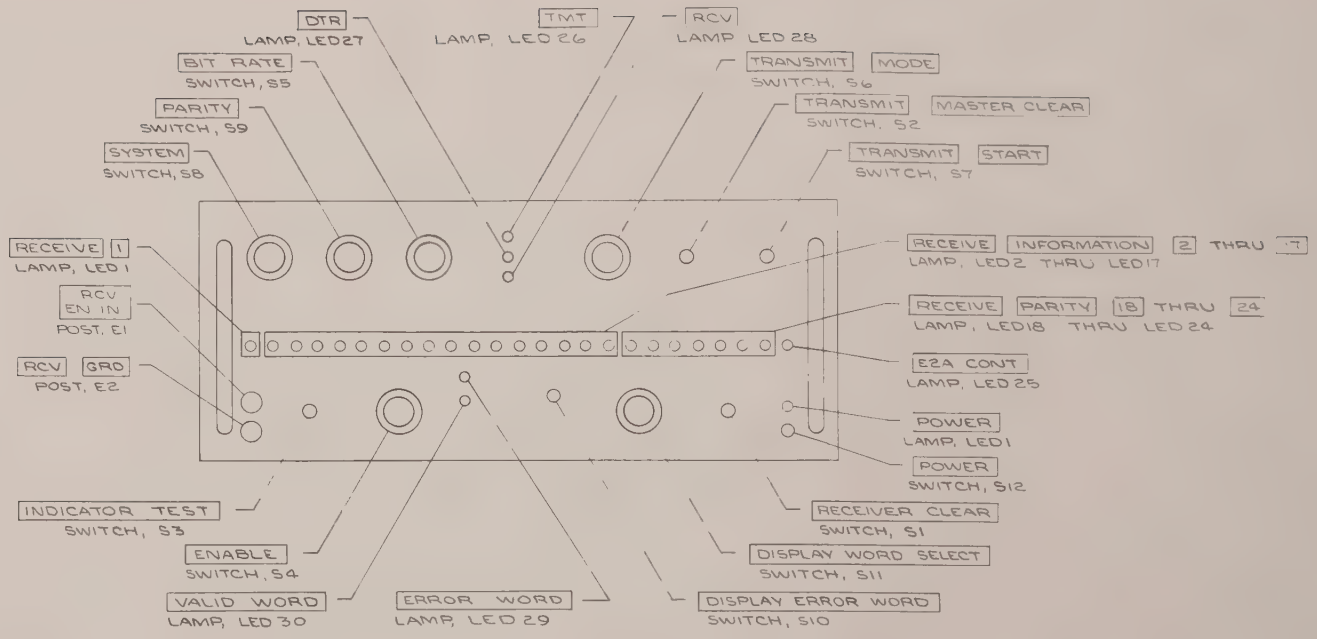
STATION	thumbwheel switch (S8A)	Programs bits 7, 8, and 9 of word 1 in all instructions with the least significant bit (LSB) being bit 7.
	thumbwheel switch (S8B)	Programs bits 4, 5, and 6 of word 1 in all instructions (LSB=bit 4).
REMOTE SWITCH	thumbwheel switch (S6A)	Programs bits 14, 15, 16 and 17 of word 1 of the REMOTE SWITCH instruction **only** (LSB=bit 17).
	thumbwheel switch (S6B)	Programs bits 2, 3, 4 and 5 of word 2 of the REMOTE SWITCH instruction **only** (LSB=bit 2).
	thumbwheel switch (S6C)	Programs bits 6, 7, 13 and 14 of word 2 of the REMOTE SWITCH instruction **only** (LSB=bit 6) and the most significant bit (MSB) is bit 4.
GROUP	thumbwheel switch (S7)	Programs bits 14, 15, 16 and 17 of word 1 of the GROUP REPORT and DISPLAY REPORT instructions. (LSB=bit 17).
DISPLAY	thumbwheel switch (S5)	Programs bits 13 and 14 of word 2 of the DISPLAY REPORT instruction. (LSB=bit 13).
ALARM REPORT	push button switch (S1) and lamp (LED 1)	Interlocked instruction switch which initiate specific instruction data formats. The lamps illuminate upon depression of their respective instruction switch.
GROUP REPORT	push button switch (S2) and lamp (LED 2)	
DISPLAY REPORT	push button switch (S3) and lamp (LED 3)	
REMOTE SWITCH	push button switch (S4) and lamp (LED 4)	
J1 connector (J1)		Permits connection (with use of an interconnecting cable) to J1 of the Basic Test Set Model 2474.

TABLE 2-4
MODEL 2477
CONTROLS, INDICATORS AND CONNECTORS

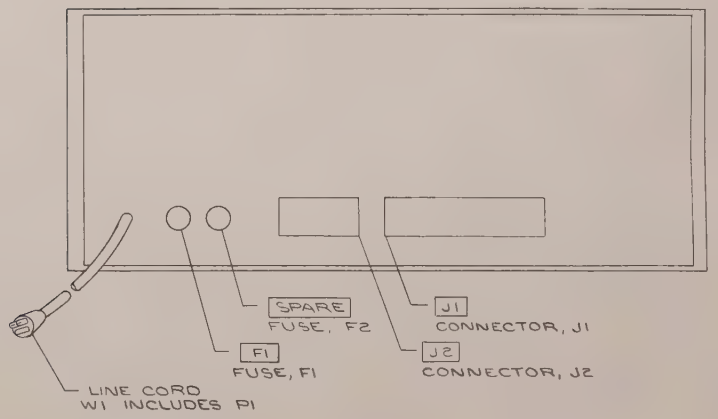
WORD 1 WORD 2 WORD 3 WORD 4	toggle switches (S1-S68)	The 68 (four 17 bit words) bit switches cause their respective bits to be a logic "1" in the up position and logic "0" in the down position.
WORD 1 WORD 2 WORD 3 WORD 4	lamps (LEDS 1-4)	These lamps illuminate when their respective word is being transmitted.
MESSAGE LENGTH WORDS	rotary switch (S70)	This control determines the number of words (1, 2, 3, 4 or 16) in the message. 16 word messages contain the 4 unique words in the following sequence: 1, 2, 3, 4, 2, 3, 4, 2, 3, 4, 2, 3, 4, 2, 3, and 4.
RCU ON/OFF	toggle switch (S69)	With this switch ON and Model 2474 in the ANSWER mode, the PI causes one of two messages to be transmitted as follows: a) STATION TEST SET (Model 2474) receives a 1 word message (bits 1, 2, 3 = 000) causing a 1 word reply message (WORD 1). b) STATION TEST SET (Model 2474) receives a 1 word message (bits 1, 2, 3 = 010) causing a 3 word reply message (WORDS 2, 3 and 4). c) STATION TEST SET (Model 2474) receives a 1 word message (bits 1, 2, 3 ≠000 or 010) causing no reply message.
J1 connector (J1)		Permits connection (with use of an interconnecting cable) to J1 of the Basic Test Set Model 2474.

TABLE 2-5
INTERCONNECTING AND TEST CABLE CONNECTORS

Interconnecting Cable (P/N 8770)	PI, PI	Provides means of connecting J1 — Model 2474 to J1 — Plug-In in use.
E1/E2 Test Cable (P/N 8592)	P2, CPb, CPc	Provides means of connecting J2 — Model 2474 to E1/E2 Station under test.
E2A Test Cable (P/N 8593)	P2, P3	Provides means of connecting J2 — Model 2474 to E2A Station under test.
E2A TCT Test Cable (P/N 8597)	P2, P3	Provides means of connecting J2 on Model 2474 to E2A Station under test.



FRONT VIEW



REAR VIEW

FIGURE 2-1
CONTROL, INDICATOR AND CONNECTOR LOCATIONS
MODEL 2474

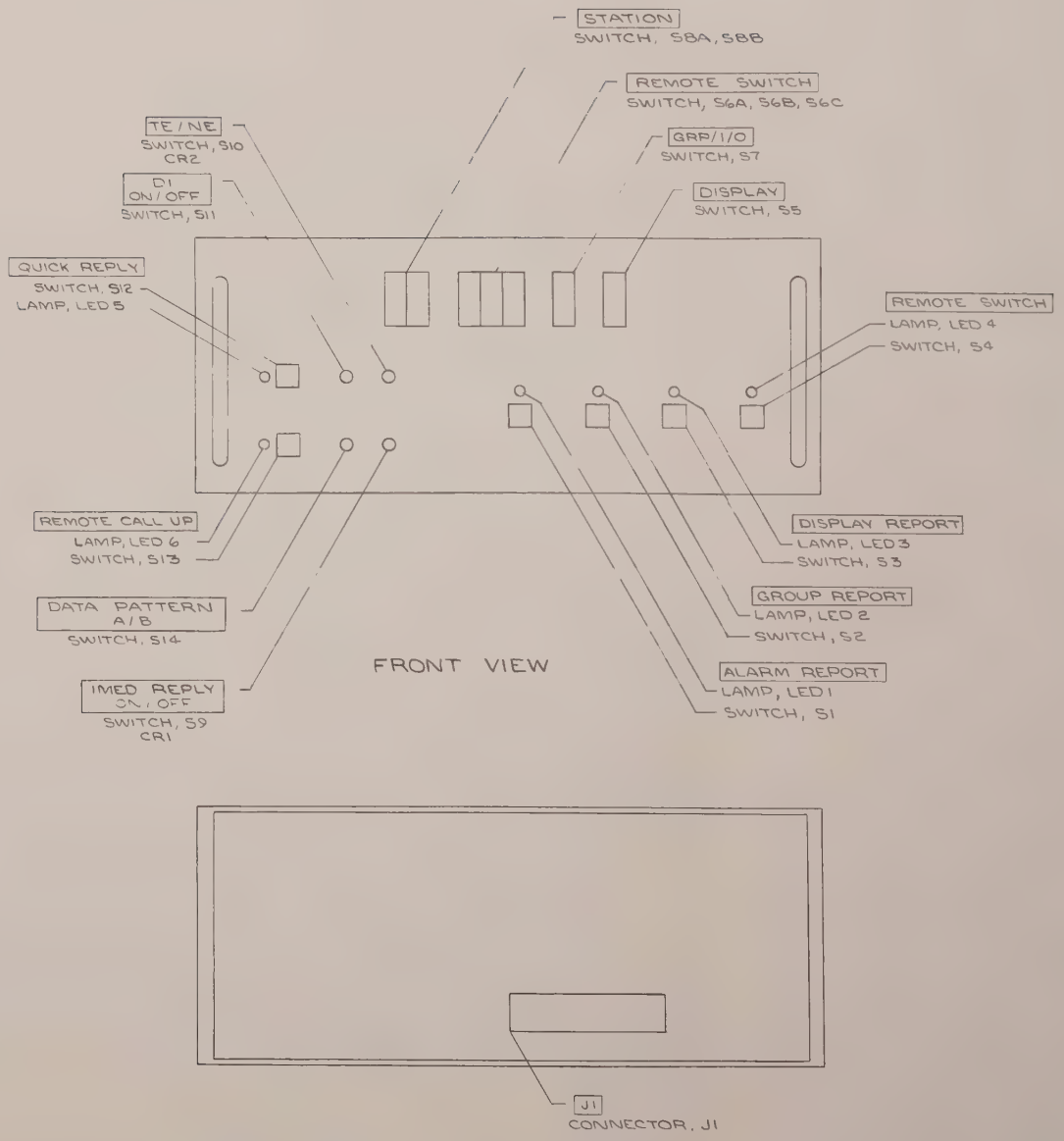


FIGURE 2-2
CONTROL, INDICATOR AND CONNECTOR LOCATIONS
MODEL 2476

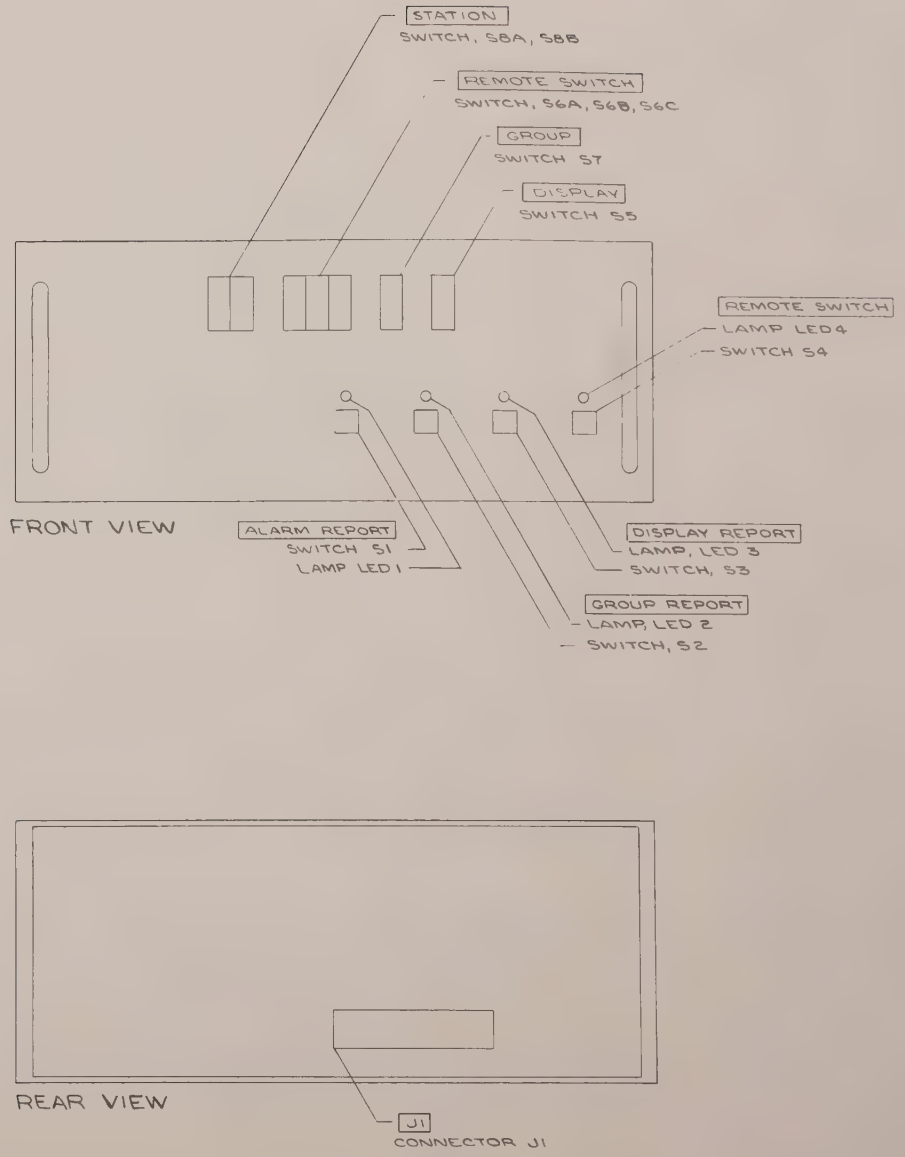
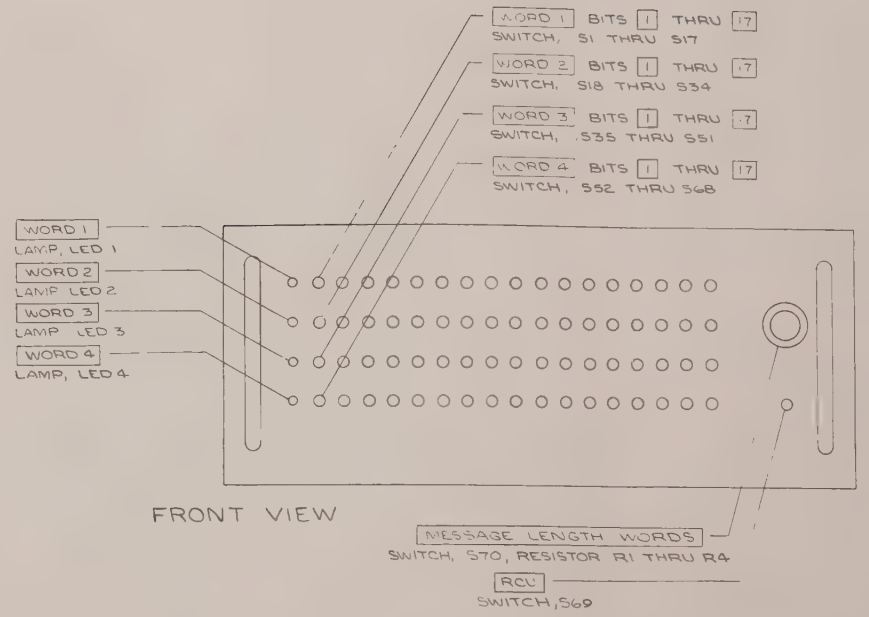


FIGURE 2-3
CONTROL, INDICATOR AND CONNECTOR LOCATIONS
MODEL 2475



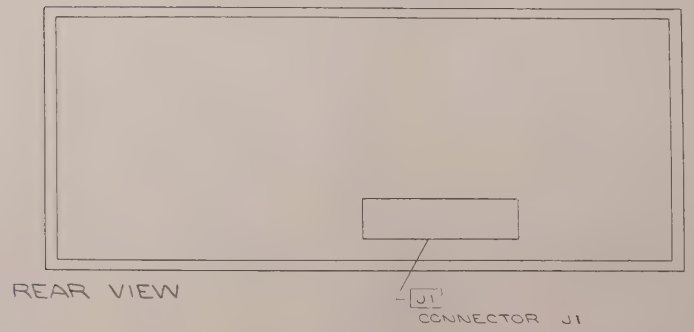


FIGURE 2-4
CONTROL, INDICATOR AND CONNECTOR LOCATIONS
MODEL 2477

Principles of Operation

3-1. INTRODUCTION

3-1a. This section consists of two parts, the first being a discussion of THEORY OF OPERATION and the second being a board by board CIRCUIT DESCRIPTION. Each part is devoted to a written description (referenced to block diagrams, waveforms, tables, data format charts and/or schematics) for each model. All diagrams, tables and charts are found in this section. Schematics are located in Section 7 "Parts Lists and Circuit Diagrams" and waveforms are located in Section 6 "Trouble Shooting." Both schematics and waveforms are presented as foldouts so that either can be viewed while reading this section.

3-2. THEORY OF OPERATION

3-2a. **Model 2474**

Refer to block diagrams Figures 3-1 and 3-2. The Model 2474 has the ability to receive, display and transmit E1/E2 and E2A Telemetry information.

The SIMPLIFIED BLOCK DIAGRAM Figure 3-1 illustrates the interaction of the Model 2474 with the E-Telemetry Station equipment and the Plug-In unit. The Master Clock Timing and Control is also shown since this block provides the clocking and controls required to implement Receive, Display and Transmit and Plug-In operation.

Front panel controls are shown as dotted lines to indicate operator controlled inputs to the various functions. The Receive and Display function includes the ability to check the validity of incoming data through parity checking and to count received words and display the contents of selected received. words. Detection of when a selected word has not been received is also provided. Display indicators provide Valid Word and Error Word information in addition to monitoring various inputs.

The Transmit function includes the ability to count transmit words and accept serial data words from the Plug-In and generate and attach parity to these words to form transmit words. The E-Telemetry to Test Set and Test Set to E-Telemetry interfaces provide level shifting to meet EIA RS-232 Standards and Basic Test Set requirements.

The expanded BLOCK DIAGRAM Figure 3-2 further defines functions included in the SIMPLIFIED BLOCK DIAGRAM.

The E-TELEMETRY TO TEST SET INTERFACE includes the following functions:

R/T CONTROL
RCV
EXTERNAL RCV
DATA TERMINAL READY
RCV INFO BITS

RECEIVE AND DISPLAY includes the following functions:

STANDBY LATCHES & GATING
RCV STANDBY CLOCK
DISPLAY INFO
VALID WORD
DISPLAY
DISPLAY CONTROL
WORD COUNTER RESET
WORD COUNTER
PARITY GENERATOR, CHECKER AND CONTROL

MASTER CLOCK AND TIMING CIRCUITS includes the following functions:

MASTER CLOCK CONTROL
MASTER CLOCK TIMING

TRANSMIT includes the following functions:

TMT CLOCK
WORD COUNTER RESET
WORD COUNTER
PARITY GENERATOR, CHECKER AND CONTROL

TEST SET TO E-TELEMETRY INTERFACE includes the following functions:

RCV DATA (RD)
CARRIER DETECT (CD) AND TONE
CLEAR TO SEND (CTS)

3-2b. **Model 2476**

Refer to block diagrams Figures 3-3 and 3-4 and tables 3-1 and 3-2. The MANUAL ALARM CENTRAL-B PI is capable of formatting 6 different instruction messages.

These instructions are initiated by pressing one of the front panel pushbutton switches. The SIMPLIFIED BLOCK DIAGRAM Figure 3-3 illustrates the interaction of the Model 2476 with the BTS Model 2474. Front panel controls are shown as dotted lines to indicate operator controlled inputs to various functions. The Instruction Control permits only one instruction to be operational at one time as determined by the Instruction Initiate Switches. Instruction Indicators associated with the Instruction Initiate Switches are controlled by the Instruction Control. INDICATOR TEST and MASTER CLEAR are provided to test and clear the Instruction Indicators, respectively. Data Select, Data Registers, and Transmit Word Select accepts Instruction Data determined by the front panel toggle switches and thumbwheel switches and stores this data in the appropriate word register to be shifted out to generate TMT INFO BITS.

The expanded BLOCK DIAGRAM Figures 3-4 further defines functions included in the SIMPLIFIED BLOCK DIAGRAM. Instruction INITIATE SWITCHES contains the following:

ALARM REPORT
GROUP REPORT
DISPLAY REPORT
REMOTE SWITCH
REMOTE CALL UP
QUICK REPLAY

INSTRUCTION DATA contains the following:

STATION
GRP/1/0
DISPLAY
REMOTE SWITCH
IMED. REPLY
TE/NE
DI
DATA PATTERN

DATA SELECT, DATA REGISTERS AND TRANSMIT WORD SELECT include the following:

WORD 1 DATA SELECT AND SHIFT REGISTER
WORD 2 DATA SELECT AND SHIFT REGISTER
REMOTE CALL UP AND WORDS 1 +
TRANSMIT WORD SELECT

INTER-LOCKED INSTRUCTION LATCHES are contained in the INSTRUCTION CONTROL so that when an instruction is initiated and latched all other instructions are disabled.

REMOTE CALL UP AND WORDS 2 + is utilized only when the REMOTE CALL UP pushbutton is depressed requiring transmission of 16 word messages. All other instructions initiate either 1 or 2 word messages. COUNTER RESET is generated at the end of each transmitted message. Tables 3-1 and 3-2 indicate the various positions of the INSTRUCTION DATA SWITCHES and the bit positions and words effected by the various INSTRUCTION DATA switches and IN— STRUCTION INITIATED SWITCHES.

3-2c. **Model 2475**

Refer to block diagrams Figures 3-5 and 3-6 and Tables 3-3 and 3-4.

The MANUAL ALARM CENTRAL — A PI is capable of formatting four (4) different instruction messages. These instructions are initiated by pressing one of the front panel pushbutton switches.

The SIMPLIFIED BLOCK DIAGRAM Figure 3-5 illustrates the interaction of the Model 2475 with the BTS Model 2474. Front panel controls are shown as dotted lines to indicate operator controlled inputs to various functions. The Instruction Control permits only one instruction to be operational at one time as determined by the Instruction Initiated Switches. Instruction Indicators associated with the Instruction Initiated Switches are controlled by the Instruction Control. INDICATOR TEST and MASTER CLEAR are provided to test and clear the Instruction Indicators, respectively. Data Select, Data Registers and Transmit Word Select accepts Instruction Data determined by the front panel toggle switches and thumbwheel switches and stores this data in the appropriate word register to be shifted out to generate TMT INFO BITS. The expanded BLOCK DIAGRAM Figure 3-6 further defines functions included in the SIMPLIFIED BLOCK DIAGRAM.

INSTRUCTION INITIATE SWITCHES contain the following:
ALARM REPORT
GROUP REPORT
DISPLAY REPORT
REMOTE SWITCH

INSTRUCTION DATA contains the following:
STATION
GROUP
DISPLAY
REMOTE SWITCH

DATA SELECT, DATA REGISTER AND TRANSMIT WORD CONTROL include the following:

WORD 1 DATA SELECT AND SHIFT REGISTER
WORD 2 DATA SELECT AND SHIFT REGISTER
TRANSMIT WORD SELECT

INTERLOCKED INSTRUCTION LATCHES are contained in the INSTRUCTION CONTROL so that when an instruction is initiated and latched all other instructions are disabled. COUNTER RESET is generated at the end of each transmitted message. Tables 3-3 and 3-4 indicate the various positions of the INSTRUCTION DATA SWITCHES and the bit position and words effected by the various INSTRUCTION DATA SWITCHES and INSTRUCTION INITIATED SWITCHES.

3-2d. **Model 2477**

Refer to block diagrams Figures 3-7 and 3-8. Model 2477 PI permits programming of 4 unique words by front panel toggle switches. Selection of either 1, 2, 3, 4 or 16 word messages and a Remote Call-Up, RCU,feature are also available on Model 2477.

TABLE 3-1
E1/E2 PLUG-IN MANUAL DATA SELECT DESIGNATIONS AND CODES FOR MODEL 2476

	CONTROL DESIGNATION	SCHEMATIC SYMBOL	DATA SYMBOL	POSITION DESIGNATIONS	NUMBER OF POSITIONS	BINARY CODE
MULTI-POSITION SWITCHES	STATION	S8A	a1	1 through 8	8	1 = 000 8 = 111
		S8B	a2	1 through 8	8	1 = 000 8 = 111
	REMOTE SWITCH	S6A	d1	1 through 16	16	1 = 0000 16 = 1111
		S6B	d2	A through S	16	A = 0000 S = 1111
		S6C	d3	1 through 16	16	1 = 0000 16 = 1111
	GRP/I/O	S7	b	1 through 16	16	1 = 0000 16 = 1111
	DISPLAY	S5	c	A through D	4	A = 00 D = 11
TOGGLE SWITCHES	DI (ON/OFF)	S11	j	ON/OFF	2	ON = 1 OFF=0
	TE/NE	S10	l	TE/NE	2	TE = 1 NE = 0
	DATA PATTERN A/B	S14	k	A/B	2	See Para. 2-4d
	IMED REPLY ON/OFF	S9	m	ON/OFF	2	ON = 1 OFF=0

Note: In lettered multi-position switch designations (I, O and Q) are not used.

TABLE 3-2
DATA FORMAT FOR MODEL 2476 P I

INSTRUCTION	WORD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
ALARM REPORT	1	0	0	0	LSB ← a2 →		MSB	LSB ← a1 →		MSB	0	0	0	0	0	0	0	0
GROUP REPORT	1	0	1	0	LSB ← a2 →		MSB	LSB ← a1 →		MSB	0	0	0	0	MSB ← b →			LSB
DISPLAY REPORT	1	0	1	1	LSB ← a2 →		MSB	LSB ← a1 →		MSB	0	0	0	0	MSB ← b →			LSB
	2	1	0	0	0	0	0	0	0	1	0	0	0	LSB ← c →	MSB	0	0	0
REMOTE SWITCH	1	0	1	1	LSB ← a2 →		MSB	LSB ← a1 →		MSB	0	0	0	0	MSB ← d1 →			LSB
	2	1	LSB ← d3 →			MSB	LSB ← d2 →		0	0	0	0	1	← d2 →	MSB	0	0	0
REMOTE CALL UP	1	1	0	0	LSB ← a2 →		MSB	LSB ← a1 →		MSB	0	0	0	m	MSB ← b →			LSB
	2 through 16	1 ← k →																
QUICK REPLY	1	1	0	0	0	0	0	0	0	0	0	0	j	l	0	0	0	0

LSB means (least significant bit)
MSB means (most significant bit)

TABLE 3-3
E1/E2 PLUG-IN MANUAL DATA SELECT
DESIGNATIONS AND CODES
FOR
MODEL 2475

	CONTROL DESIGNATION	SCHEMATIC SYMBOL	DATA SYMBOL	POSITION DESIGNATIONS	NUMBER OF POSITIONS	BINARY CODE
MULTI-POSITION SWITCHES	STATION	S8A	a1	1 through 8	8	1 = 000 8 = 111
		S8B	a2	1 through 8	8	1 = 000 8 = 111
	REMOTE SWITCH	S6A	d1	1 through 16	16	1 = 0000 16 = 1111
		S6B	d2	A through S	16	A = 0000 S = 1111
		S6C	d3	1 through 16	16	1 = 0000 16 = 1111
	GROUP	S7	b	1 through 16	16	1 = 0000 16 = 1111
	DISPLAY	S5	c	A through D	4	A = 00 D = 11

Note: In lettered multi-position switch designations (I, O and Q) are not used.

TABLE 3-4
DATA FORMAT FOR MODEL 2475 P I

INSTRUCTION	WORD	1	2	3	4	5	6	BITS 7	8	9	10	11	12	13	14	15	16	17
ALARM REPORT	1	0	0	0	LSB ← a2		MSB →	LSB ←	a1	MSB →	0	0	0	0	0	0	0	0
GROUP REPORT	1	0	1	0	LSB ← a2		MSB →	LSB ←	a1	MSB →	0	0	0	0	MSB ← b →			LSB
DISPLAY REPORT	1	0	1	1	LSB ← a2		MSB →	LSB ←	a1	MSB →	0	0	0	0	MSB ← b →			LSB
	2	1	0	0	0	0	0	0	0	1	0	0	0	LSB ← C →	MSB	0	0	0
REMOTE SWITCH	1	0	1	1	LSB ← a2		MSB →	LSB ←	a1	MSB →	0	0	0	0	MSB ← d1 →			LSB
	2	1	LSB ← d3			MSB →	LSB ← d2 →		0	0	0	0	1	← d2 →	MSB	0	0	0

LSB means (least significant bit)
MSB means (most significant bit)

The SIMPLIFIED BLOCK DIAGRAM Figure 3-7 illustrates the interaction of the Model 2477 with the BTS Model 2474. Front panel controls are shown as dotted lines to indicate operator controlled inputs to various functions. The Word Registers accept information from the Word Bit Switches. Transmit Word Select generates TMT INFO BITS by selecting the outputs from the Word Registers as a function of MESSAGE LENGTH WORDS 1, 2, 3, 4, 16 or RCU A, B, C in the event that RCU ON, OFF is ON.

The expanded BLOCK DIAGRAM Figure 3-8 further defines functions included in the SIMPLIFIED BLOCK DIAGRAM.

WORD BIT SWITCHES includes the following:

WORD 1 (BITS 1-17)
WORD 2 (BITS 1-17)
WORD 3 (BITS 1-17)
WORD 4 (BITS 1-17)

WORD REGISTERS contains the following:

WORD 1 SHIFT REGISTER
WORD 2 SHIFT REGISTER
WORD 3 SHIFT REGISTER
WORD 4 SHIFT REGISTER
PAR/SER CLOCK

TRANSMIT WORD SELECT contains the following:

TRANSMIT WORD SELECT SWITCH
WORD 1 CONTROL
WORDS 2, 3, 4 CONTROL
COUNTER RESET
REMOTE CALL UP CONTROL
TRANSMIT WORD RECLOCK
TRANSMIT WORD INDICATOR DRIVE

The output from the Transmit Word Select Switch depends on the state of the Word 1 Control and Word 2, 3, 4 Control. If the RCU Switch is ON the control levels are determined by RCU A, B, C. If the RCU Switch is OFF these levels are determined by the Word Counter A, B, C, D and Message Length Words 1, 2, 3, 4, 16. The output of the Transmit Word Select Switch is reclocked to generate TMT INFO BITS. INDICATOR TEST and $\overline{\text{TMTL}}$ provide for testing the TRANSMIT WORD INDICATORS and lighting them only when transmitting. COUNTER RESET is generated at the end of each transmitted message.

3-3. CIRCUIT DESCRIPTION

3-3a. **Model 2474 Circuitry**

1) RECEIVE LOGIC - BOARD 9001

Refer to Figure 7-6 for schematic information and Figure 6-1 for pertinent waveforms.

The RECEIVE LOGIC board performs the following functions:

Generates DISPLAY INFO
Generates WORD COUNTER RESET
Generates RCV/STANDBY CLK

a) DISPLAY INFO GENERATION

DISPLAY INFO can either be RCV INFO BITS, zeros or ones. Zeros are displayed by pressing either MASTER CLEAR or RECEIVER CLEAR. Ones are displayed by pressing INDICATOR TEST. DISPLAY INFO is generated by FLIP-FLOPS IC1A, IC1B, and IC2A, NOR GATES IC5A, IC5B and IC5D and EXCLUSIVE OR GATE IC6A. RCV INFO BITS from Interface II, Board 9008, at Pin S(15) is normally inverted first by IC5B and secondly by IC5D to generate DISPLAY INFO at the output of IC5D. This occurs since [MASTER CLEAR + RECEIVER CLEAR] at IC6A , Pin 11 and INDICATOR TEST, 2475, 2476 at IC2A, Pin 13 are normally logic 0. Pressing the MASTER CLEAR button (S2) Pin U (17) causes the Q output of IC1B to be logic 1. Likewise the Q output of IC1A will be logic 1 if the RECEIVER CLEAR button (S1) Pin V(18) is pressed. If either of these Q terminals is at logic 1 then the output of IC5A is at logic 0 and the output of IC6A, MASTER CLEAR or RECEIVER CLEAR is at logic 1. [MASTER CLEAR + RECEIVER CLEAR] at logic 1 applied to IC5D causes DISPLAY INFO to be zeros. Pressing the INDICATOR TEST button (S3) Pin X(20) causes the Q terminal of IC2A to be logic 1 and in turn the output of IC5B to be logic 0. This logic 0 applied to IC5D causes DISPLAY INFO to be ones. When the Q terminal of either IC1A, IC1B, or IC2A goes to logic 1 a word cycle is initiated. At the end of the word cycle the Q terminal at logic 1 will reset to logic 0 by B GATE MONO at Pin W(19), a pulse approximately 70 usec wide occurring at the end of every word cycle. If either of the buttons is pressed the output of NOR GATE IC5C will be logic 0 and the output of EXCLUSIVE OR GATE IC6B [MASTER CLEAR + RECEIVER CLEAR + INDICATOR TEST] will be logic 1 for one word cycle.

[MASTER CLEAR + RECEIVER CLEAR] present at Pin B(2) goes to Board 9004 Pin K(9) where it is used to reset various circuitry. DISPLAY INFO present at Pin R(14) goes to Board 9010 Pin Y(2I) where the information is displayed. MASTER CLEAR at Pin U(17) also goes to Board 9003 Pin E(5) to initially reset various circuitry. INDICATOR TEST at Pin X(20) goes to Board 9010 Pin E(5) for testing indicators and also provides an interruptable ground connection for the SYSTEM switch.

b) WORD COUNTER RESET Generation

The WORD COUNTER RESET, Pin L(10), at logic 1 will cause the word counter to be reset to state 0. WORD COUNTER RESET will go to logic 1 if COUNTER RESET from PI Pin N(12), R/T CONTROL Pin D(4), ERROR STROBE Pin E(5) or [MASTER CLEAR + RECEIVER CLEAR + INDICATOR TEST] goes to logic 1. WORD COUNTER RESET is generated by NOR GATES IC3A, IC3B, and IC3C, EXCLUSIVE OR GATE IC6D and OR GATE comprised of CR3, CR4 and R9. If either ERROR STROBE or $\overline{\text{R/T CONTROL}}$ goes to logic 1 then the output of IC3A will go to logic 0 and the

output of IC3B will go to logic 1. Logic 0 to logic 1 transitions at IC3B Pin 4 will be differentiated by C2 and R6 and applied to IC3C. [MASTER CLEAR + RECEIVER CLEAR + INDICATOR TEST] is also applied to IC3C. If either input goes to logic 1 then IC3C Pin 10 goes to logic 0. This signal is delayed by R8 and C3 and inverted by IC6D to generate one input to the 2 input discrete OR GATE, the other input being COUNTER RESET from the PI. If either one of these two inputs goes to logic 1 then WORD COUNTER RESET goes to logic 1. COUNTER RESET present at Pin N(12) is also applied to Board 9003 Pin C(3) and Board 9007 Pin F(6). WORD COUNTER RESET is applied to Board 9006 Pin B(2).

c) $\overline{\text{RCV/STANDBY CLK}}$ Generation

$\overline{\text{RCV/STANDBY CLK}}$ transitioning from logic 1 to logic 0 initiates a word cycle upon pressing of MASTER CLEAR, RECEIVER CLEAR or INDICATOR TEST or upon presence of a sync bit on the RCV INFO BITS line. $\overline{\text{RCV/STANDBY CLK}}$ is generated by FLIP-FLOPS IC4A, IC4B and IC2B, NOR GATES IC7A, IC7B, IC7C, IC7D and IC3D, EXCLUSIVE OR GATE IC6C and OR GATE comprised of CR1, CR2, CR5 and R7. When either of the above push buttons are pressed [MASTER CLEAR + RECEIVER CLEAR + INDICATOR TEST] will transition from logic 0 to logic 1. This applied to IC3D will cause the output of IC3D to properly transition and initiate a word cycle since the other input to IC3D is normally logic 0. When receiving, the presence of a sync bit on the RCV INFO BITS line produces a logic 0 to logic 1 transition at the CK terminal of IC2B. This transition will make the Q output of IC2B logic 1 only if the R terminal of IC2B is held at logic 0 thereby causing the $\overline{\text{RCV/STANDBY CLK}}$ line to initiate a word cycle.

The output of IC7D applied to IC6C determines the state of the R terminal of IC2B since the other input to IC6C, namely B GATE MONO, is normally logic 0. If the output of IC7D is logic 0 then the R terminal is logic 0 and IC2B is able to transition due to a sync bit. If the output from IC7D is logic 1 then the R terminal is logic 1 and IC2B is held in its reset state and reception is inhibited. With the RECEIVE ENABLE Switch in the NORMAL position Pin K(9) is at logic 1 causing the outputs of IC7A and IC7B to be at logic 0. The output of IC7C is logic 1 since the normal state of ERROR LATCH is logic 0. This makes the output of IC7D logic 0 thereby enabling IC2B. With the RECEIVE ENABLE Switch in either position +EXT or —EXT the output of IC7C is logic 0 since the output of IC7A is logic 1 due to Pin K(9) being logic 0. The output of IC7B is now determined by IC4B. Since the normal state of IC4B is $\overline{Q}$ at logic 1 then the output of IC7B is logic 0 and the output of IC7D is logic 1 inhibiting IC2B and preventing reception. When RCV EXT CLK Pin J(8) from Board 9008 is present at the CK terminal of IC4B $\overline{Q}$ is driven to logic 0, the output of IC7B goes to logic 1 making the output of IC7D logic 0. This enables reception of the next message. At the end of the received message the $\overline{\text{R/T CONTROL}}$ line transitions from logic 0 to logic 1 resetting IC4B by way of CR2 and R7 to its normal state. If ERROR STROBE Pin E(5) appears at the CK terminal of IC4A then ERROR LATCH is driven to logic 1. When this occurs during normal enabled reception the output of IC7D will go to logic 1 inhibiting reception since the output of IC7C goes to logic 0. When this occurs during external enabled reception the output of IC7D will also go to logic 1 since IC4B $\overline{Q}$ is held at logic 1 by way of CR5 and R7 driving the output of IC7B to logic 0. Reception can only be enabled by pressing MASTER CLEAR or RECEIVER CLEAR thereby resetting IC4A. ERROR STROBE is generated if a parity error is detected and the DISPLAY ERROR WORD Switch is ON. [MASTER CLEAR + RECEIVER CLEAR] also resets IC4B by way of CR1 and R7. EXT RCV Pin H(7) is selected in external enabled receive by S4C and applied to Board 9003 Pin S(15) and DISPLAY ERROR WORD Switch.

2) MASTER CLOCK - BOARD 9002

Refer to Figure 7-7 for schematic information and Figfure 6-1 for pertinent waveforms.

The MASTER CLOCK board performs the following functions:
Generate MASTER CLOCK
Generate Control Signals

a) MASTER CLOCK Generation

The MASTER CLOCK frequency is determined by the position of the BIT RATE switch (S5). In the 150 BITS/SEC, 600 BITS/SEC and 1200 BITS/SEC positions the MASTER CLOCK will be 150 Hz, 600 Hz and 1200 Hz, respectively. The MASTER CLOCK is generated by dividing the output of a 153.6 KHz crystal oscillator by 64, 128 and 512, then selecting either 2400 Hz, 1200 Hz or 300 Hz, using the BIT RATE switch, and dividing by 2 thereby generating either 1200 Hz, 600 Hz or 150 Hz.

The crystal oscillator consists of DUAL COMPLEMENTARY pairs IC1A, IC1B, crystal Y1, R1, R2 and C1. IC1A and R1 combined form the oscillator amplifier section of the crystal oscillator with a 180° phase shift between input Pin 6 and output Pins 8, 13 of IC1A. IC1B, Y1, C1 and R2 form the feedback section of the Crystal Oscillator. This section provides the additional 180° phase shift required to sustain oscillations. IC1B also serves as a buffer so that minimal loading effects are observed when the crystal oscillator is connected to the frequency dividing networks. Hence the output of this circuit is taken from Pins 1, 5 of IC1B and is a square wave of 50% duty cycle varying between zero and +5 v at 153.600 KHz. R2 and C1 provide additional compensation for any added phase shift due to crystal Y1.

The 153.600 KHz clock from the Crystal Oscillator is applied to the clock input of a 12 STAGE RIPPLE CARRY BINARY COUNTER/DIVIDER IC2. Three divided down outputs of 2400, 1200 and 300 Hz are obtained at Pins 2, 4, and 12 of IC2 respectively and are fed to three of four inputs of a QUAD BILATERAL SWITCH IC3. The output of IC3 is determined by the BIT RATE switch position placing a logic 1 at either IC3 C, B or D terminals in positions 1200, 600 or 150, respectively. The output of IC3 is then fed to EXCLUSIVE OR GATE IC4A to be passed unaltered or inverted if the R/T CONTROL is logic 0 or logic 1 (Receive), respectively. The output of IC4A is then divided by 2 by FLIP FLOP IC5A to generate the appropriate MASTER CLOCK at Pin L(10). MASTER CLOCK is utilized on Boards 9004, 9005 and 9007 and by the PI unit.

b) CONTROL SIGNAL GENERATION

Control signals are generated by DECADE COUNTER-DIVIDER IC6, EXCLUSIVE OR GATES IC4B, C and D and FLIP-FLOPS IC7A and B, IC8A and B and IC5B. The control signals generated are "A" GATE Pin J(8) (18 bits corresponding to sync bit and 17 information bits), B GATE Pin H(7) (7 bits corresponding to 7 parity bits), "B" GATE PLUG IN (PI) Pin N(12) ("B" GATE modified by TMTL), $\overline{26\ RESET}$ Pin K(9) (a down clock occurring 1 count after the B GATE) and COUNT 4 Pin C(3) (1 count wide pulse occurring once per cycle of IC6). The timing of these control signals when compared to the MASTER CLOCK can vary three ways depending on the states of R/T CONTROL, MASTER CLOCK START and MASTER CLOCK CONTROL. The states of these signals depend on whether the test set is receiving or transmitting, the position of the SYSTEM switch and, if transmitting, the word being transmitted. In standby the Q outputs of IC7A and B, IC8A and B and IC5B are at logic 1 and IC6 is held reset. Since the Q outputs of IC7B and IC8B are applied to IC4D the output of IC4D("A" GATE) is at logic 0. Likewise the output of IC4C ("B"GATE) is also at logic 0 since the Q outputs of IC7B and IC8A are applied to IC4C. In standby the Q output of IC5B is prevented from holding IC2 and IC5A reset since R/T CONTROL is at logic 0 holding the resets to IC2 and IC5A to logic 0 through R6 and CR1. This permits generation of MASTER CLOCK. IC8B is likewise prevented from being set by MASTER CLOCK because of CR2 and R8. When receiving the R/T CONTROL goes to logic 1 thereby allowing the Q output of IC5B to hold IC2 and IC5A reset preventing generation of MASTER CLOCK and allowing IC8B to be set by MASTER CLOCK. The MASTER CLOCK START Pin D (4) and MASTER CLOCK CONTROL Pin B(2) are pulsed on detecting the presence of a sync bit. This resets the Q outputs of IC7A and B. IC8A and B and IC5B to logic 0 thereby allowing IC2 and IC5A to operate generating MASTER CLOCK. Since the inputs to IC4C and IC4D are still at the same logic level "A" GATE and "B" GATE remain at logic 0. MASTER CLOCK goes to logic 1 1/2 bit later setting the Q output of IC8B and one input to IC4D to logic 1 thereby causing the "A" GATE and D input of IC7A to go to logic 1 and resetting IC6 through C2 and R7. IC6 now counts up to 9, at which time the logic 1 D input of IC7A is transferred to its Q output and D input of IC7B. IC6 continues to count to 18 at which time the logic 1 D input to IC7B is transferred to its Q output and D input of IC8A, causing the "A" GATE to drop to logic 0 and the "B" GATE to go to logic 1. IC6 continues to count to 25 at which time the logic 1 D input to IC8A is transferred to its Q output and the D input of IC5B, causing "B" GATE to return to logic 0. The MASTER CLOCK advances one additional count transferring the logic 1 D input to IC5B to its Q output forcing $\overline{26\ RESET}$ at Pin K (9) to logic 0. This logic 1 returns IC2 and IC5A to a reset condition terminating the word cycle until the next sync bit is received. When referring to Figure 6-1 IC6 counts of 9, 18, and 25 correspond to MASTER CLOCK positive edges numbered 10, 19, and 26 respectively. Since the "A" GATE starts 1/2 bit after detection of a sync bit the incoming data is sampled at the half bit position. When transmitting the MASTER CLOCK is free running as previously described under standby conditions since R/T CONTROL is at logic 0 during transmit. The previously described sequence differs in the following manner when transmitting:

1. When transmitting E1/E2 words or Word 1 E2A IC8B remains reset after the occurrence of MASTER CLOCK CONTROL and MASTER CLOCK START until IC6 counts to 7, at which time IC8B Q output goes to logic 1 initiating "A" GATE and starting the timing sequence.

2.When transmitting words greater than 1 E2A the Q output of IC8B is always at logic 1 since only MASTER CLOCK START is applied causing "A" GATE to be logic 1 when IC7B is reset and starting the timing sequence. "B" GATE is modified by TMTL using CR3 and R9 to generate "B" GATE PI. This control signal required by the PI prevents cycling of the PI except when transmitting.

3) TRANSMIT LOGIC - BOARD 9003

Refer to Figure 7-8 for schematic information and Figure 6-3 for pertinent waveforms.

The Transmit Logic board performs the following functions:

Generate MASTER CLOCK START and CONTROL - Generate TMT CLK -

a) MASTER CLOCK START and CONTROL GENERATION

The MASTER CLOCK START, Pin D(4), at logic 1 for approximately 100 usec will initiate the Master Clock, Board 9002, to cycle through 1 word. Start pulses are generated by FLIP-FLOP IC5B either by setting IC5B by [TMT CLK + RCV/STANDBY CLK] transitions from logic 0 to logic 1, or by clocking IC5B by pressing the MASTER CLEAR button (S2) Pin E(5). [TMT CLK +

RCV/STANDBY CLK] is generated by OR GATE comprised of CR12, CR13, and R17. MASTER CLEAR is applied directly to IC5B to permit clearing should the flip-flops on Board 9001 initially prevent RCV/STANDBY CLK from starting the MASTER CLOCK and clearing the test set.

When transmitting, the MASTER CLOCK CONTROL, Pin B (2), will either be identical to MASTER CLOCK START or held at logic 0 to delay the start of the A GATE by 7 bits, or 0 bits from the MASTER CLOCK START, respectively. This control depends on the position of the system switch and whether the test set is transmitting Word 1 or words greater than one, as follows:

In E1/E2 transmit the MASTER CLOCK CONTROL is the same as MASTER CLOCK START regardless of transmitted word.

In E2A transmit, Word 1, the MASTER CLOCK CONTROL is the same as MASTER CLOCK START.

In E2A transmit, Words 2, 3, etc., the MASTER CLOCK CONTROL is logic 0.

The output of NOR GATE IC6C controls the generation of MASTER CLOCK CONTROL at NOR GATE IC6D. If the System Switch (S8) Pin L(10) is in the E1/E2 position the output of IC3A is logic 1 making the output of IC6C logic 0. The output of IC6C logic 0 applied to IC6D satisfies above condition 1. In switch position E2A the output of IC3A is logic 0 enabling the IC6C to invert $\overline{\text{TMTL}}$ delayed by R16 and C9 to inhibit IC6D after word 1 MASTER CLOCK START to satisfy conditions 2 and 3.

When receiving MASTER CLOCK CONTROL will always be the same as MASTER CLOCK START since $\overline{\text{TMTL}}$ is always logic 1 causing the output of IC6C to be logic 0 enabling IC6D.

b) TMT CLK GENERATION

TRANSMIT CLK is generated by NOR GATE IC6B. Transitions from logic 0 to logic 1 of TRANSMIT CLK will generate a MASTER CLOCK START pulse as previously described. At the start of each transmitted message FLIP-FLOP IC5A is clocked either by pressing the START button (S7) Pin H(7) in all Transmit Modes, or by COUNTER RESET Pin C(3) appropriately delayed in the CONTINUOUS MODE by Timer IC1 or by logic 1 to logic 0 transitions at Pin S (15) in the ANSWER MODE. This OR GATE is comprised of CR6, CR7, CR8 and R14. The input at Pin S (15) comes from the ENABLE SWITCH (S4). In the NORMAL position the input is R/T CONTROL and in the +EXT or -EXT position the input is EXT RCV. IC5A is reset either by pressing the MASTER CLEAR button or COUNTER RESET generated in the PI or held reset by TMT INHIBIT Pin F(6) under certain Model 2477 RCU ANSWER conditions. This OR GATE is comprised of CR9, CR10, CR11 and R15.

The $\overline{Q}$ output of IC5A, when clocked, will transition from logic 1 to logic 0 thus enabling NOR GATE IC6B and generating a TMT CLK corresponding to Word 1. IC6B, now enabled, inverts the output of NOR GATE IC4D to generate TMT CLK corresponding to Words 2, 3, 4, etc. INVERTERS IC3B, IC3A and NOR GATES IC4A, IC4B, IC4C and IC4D apply B GATE MONO Pin N(12) in E1/E2 and $\overline{26\ \text{RESET}}$ Pin K(9) in E2A to IC6B to generate TMT CLK for words greater than one. $\overline{26\ \text{RESET}}$ is differentiated by C6 and R11.

In the CONTINUOUS MODE FLIP-FLOP IC5A is clocked by COUNTER RESET delayed depending on position of BIT RATE Switch S(5) to start messages 2, 3, 4, etc. The delays, generated by TIMER IC1, are 0.5 sec. in the 1200 bit rate determined by R1, R3 and C1, 2 sec., in the 600 bit rate determined by R2, R3, and C1, and 6 sec. in the 150 bit rate determined by R3 and C1. The output of IC1 is inverted by IC3D and differentiated by C8 and R13 and then applied to CR6.

NOR GATES IC2C and IC2D form a Set Reset FLIP-FLOP that terminates CONTINUOUS transmit the moment the MASTER CLEAR is depressed by holding the input to IC3D at logic 1 using OR GATE comprised of CR4, CR5 and R12.

The $\overline{Q}$ output of IC5A and COUNTER RESET are applied to NOR GATE IC6A to generate $\overline{\text{TMTL}}$ Pin J(8). $\overline{\text{TMTL}}$ is then inverted by INVERTER IC3F to generate TMTL Pin R(14). TMTL goes to logic 1 only when transmitting. The MODE Switch (S6) Pins W(19) and U(17) controls clocking of IC5A by enabling NOR GATE IC2A to invert COUNTER RESET in CONT and by enabling NOR GATE IC2B to invert the input to Pin S(15) differentiated by C2 and R5 and hold the input to IC2A at logic 0 through CR3 and ANS. In the ONCE position both IC2A and B are inhibited.

The Transmit Logic board also contains push button switch bounce suppression. R7, R8, R9, C3 and C4 provide this suppression for the START Switch and prevent a level from being held at CR8 if the START button is held pressed. R10 and C5 provide bounce suppression for the MASTER CLEAR Switch.

4) PARITY GENERATOR/CHECKER AND CONTROL — BOARD 9004

Refer to Figure 7-9 for schematic information and Figure 6-4 for pertinent waveforms.

The PARITY GENERATOR/CHECKER AND CONTROL Board performs the following functions:

Parity Generation and Checking -
Generation of TMT WORD -

a) Parity Generation and Checking

Parity generation is required in both receive and transmit. In receive parity generation results in parity checking the incoming data, RCV INFO BITS, to determine

incorrect data. In transmit, parity generation results in 7 parity bits being added to 17 TMT INFO BITS to generate TMT WORD.

The 7 parity bits are generated from the 17 information bits resulting in a 24 bit word which is an element of a set of code words defined by a 63 bit Bose — Chaudhure — Hocquerghen (BCH) code modified to 24 bits. Two parity options are provided. They are:

Parity A - 7 parity bits generated from the 17 information bits.

Parity B - parity generation is the same as for parity A except that bit 18, the first parity bit, is inverted. This is designated as a "virtual bit" added.

TABLE 3-5 PARITY BIT GENERATION indicates the 7 parity bits generated when a single one is placed in bit position 1-17 for parity A and parity B.

Parity is generated by 4 BIT SHIFT REGISTERS IC8 and IC9, EXCLUSIVE OR GATES IC1B, IC1C, and IC1D, NAND GATES IC4D and IC2D, AND GATE IC3D and MONOSTABLE MULTIVIBRATORS IC7A and B. When clocked the Q output of IC7A will go to logic 1 for approximately 70 usec determined by C11 and R11. The Q output of IC7B will go to logic 1 for approximately 7 usec determined by R12 and C 12 when clocked.

Buffered "A" GATE, "A" GATE B, Pin X(20) is inverted by IC2D and applied to IC7A. The Q output of IC7A is applied to the M terminal of IC8 and IC9. The $\overline{Q}$ output of IC7A is applied to IC7B. The Q output of IC7B provides the downclock required to load either 7 zeros or 6 zeros and a one, Parity A or Parity B, respectively into IC8 and IC9. The Q output of IC7A holds the M inputs to IC8 and IC9 to logic 1 at the downclock. The Parity Switch (S9) Pin N(12) determines the parity being generated. IC1B, IC1C and IC1D perform a modulo 2 addition of B and D outputs of IC8, C output of IC9 and TMT INFO BITS in transmit generating 7 parity bits at IC1D output during the B GATE. When transmitting the R/T CONTROL Pin S(15) at logic 0 makes $\overline{\text{R/T CONTROL}}$ Pin U(17) the output of NAND GATE IC2A logic 1. This enables AND GATE IC3A to pass "A" GATE B therefore enabling NAND GATE IC4A to invert TMT INFO BITS Pin Y(2I). The output of IC4A is inverted by IC4D and presented to IC1C since R/T CONTROL at logic 0 holds the output of IC2B at logic 1. In receive DISPLAY INFO D is added instead of TMT INFO BITS producing parity check results at the output of IC1D. DISPLAY INFO D when receiving is the same as RCV INFO BITS. R/T CONTROL at logic 1 enables IC2B and inhibits IC4A thereby passing DISPLAY INFO D to IC1C. In receive, R/T CONTROL at logic 0, parity mischecks at the output of IC1D enable NAND GATE IC5B to pass inverted MASTER CLOCK present at the output of NAND GATE IC5A only when buffered "B" GATE "B", GATE B, Pin T(16) is at logic 1. MASTER CLOCK at output of IC5B is delayed by R6 and C7 and allowed to clock FLIP-FLOP IC6B causing the Q output, ERROR WORD Pin E(5), to be logic 1 and ERROR WORD Pin F(6) to be logic 0. IC6B will either be reset by [MASTER CLEAR + RECEIVER CLEAR] Pin K(9) or the trailing edge of the following "A" GATE B utilizing OR GATE comprised of CR1, CR2, and R4. A GATE B present at the output of IC2D is differentiated by C5 and R3. R5 and CR3 prevent IC6B from being reset when TMTL Pin J(8) is logic 0. If a word selected for display has not been received then RCV WORD Pin B(2) will set IC6B Q output to logic 1. MASTER CLOCK Pin V(18) is buffered by AND GATE IC3C. EXCLUSIVE OR GATE IC1A generates A+B GATE Pin W(19) from "A" GATE B and "B" GATE B.

b) TMT WORD Generation

TMT INFO BITS Pin Y(21) are present at NAND GATE IC4A and parity bits are present at NAND GATE IC4B. IC4A is enabled by the output of AND GATE IC3A [A GATE B·$\overline{\text{R/T CONTROL}}$] and IC4B is enabled by the output of IC3B [B GATE B·$\overline{\text{R/T CONTROL}}$]. $\overline{\text{R/T CONTROL}}$ is logic 1 in transmit or standby. IC4A and IC4B outputs are fed to NAND GATE IC4C whose output [TMT INFO BITS + PARITY] is then fed to FLIP-FLOP IC6A to be reclocked by MASTER CLOCK at the output of AND GATE IC3C delayed by R2 and C4 to form TMT WORD Pin H(7). IC6A is reset by MASTER CLOCK START Pin D(4) and set by $\overline{\text{TMTL}}$ Pin J(8).

5) $\overline{\text{RCV WORD}}$/BUFFER - BOARD 9005

Refer to Figure 7-10 for schematic information and Figure 6-5 for pertinent waveforms.

The $\overline{\text{RCV WORD}}$/BUFFER board performs the following functions:

Generation of $\overline{\text{RCV WORD}}$
Generation of DISPLAY STROBE and DISPLAY RESET
Generation of VALID WORD
Buffer Control Signals

a) $\overline{\text{RCV WORD}}$ Generation

$\overline{\text{RCV WORD}}$ is generated at the end of a received message if the message length is less than the word selected for display. However, should the message contain errors and the DISPLAY ERROR WORD switch is ON the $\overline{\text{RCV WORD}}$ will not be generated.

$\overline{\text{RCV WORD}}$ Pin B(2) is generated by NOR GATES IC2C,IC2D, and FLIP-FLOPS IC3A and IC3B. IC3B operates as a monostable generating a negative pulse at $\overline{Q}$, approximately 60 usec. wide, with every negative transition of R/T CONTROL, Pin S(15). The output from IC3B goes to IC2D. IC2D will either be inhibited or enabled by IC3A. IC3A, when reset, will enable IC2D unless clocked by [SELECTED STROBE + ERROR STROBE] with the R/T CONTROL at logic 1. IC3A is reset by positive transitions at Pin K(9) differentiated by C4 and R5 caused by [MASTER CLEAR + RECEIVER CLEAR] when the DISPLAY ERROR WORD Switch S(10) is ON. When DISPLAY ERROR WORD Switch is

TABLE 3-5 – PARITY BIT GENERATION

BIT LOCATION	PARITY A	PARITY B
	BITS 18 through 24	BITS 18 through 24
0	0000000	0110010
1	0011001	0101011
2	1011000	1101010
3	0101100	0011110
4	0010110	0100100
5	0001011	0111001
6	1010001	1100011
7	1111100	1001110
8	0111110	0001100
9	0011111	0101101
10	1011011	1101001
11	1111001	1001011
12	1101000	1011010
13	0110100	0000110
14	0011010	0101000
15	0001101	0111111
16	1010010	1100000
17	0101001	0011011

Note: The procedure for determining the parity of any word is as follows:

1. Select from above table the parity associated with each logic 1 bit position.
2. Perform Modulo 2 addition with selected parity groups, that is, binary addition without carry.
3. Example – Determine Parity B for word having all zeros except for bits 1, 5 and 9.
   Bit 1 – 0101011
   Bit 5 – 0111001
   Bit 9 – 0101101
   0111111 – Calculated Parity.

OFF positive transitions at Pin K(9) will be due either to R/T CONTROL or EXT RCV depending on the position of the ENABLE Switch (S4).

IC3A will be clocked by SELECTED STROBE or ERROR STROBE if the selected word is present or error words exist and the DISPLAY ERROR WORD Switch is ON, respectively. NOR GATE IC2C inverts R/T CONTROL. C5 and R6 differentiate the output of IC2C.

b) DISPLAY STROBE and DISPLAY RESET Generation

DISPLAY STROBE Pin D(4) is required to update periodically the displayed data. DISPLAY STROBE consisting of [SELECTED STROBE + ERROR STROBE + $\overline{\text{RCV WORD}}$] is generated by CR4, CR5, and R9.

DISPLAY RESET Pin Y(21) resets the display registers to logic 0. DISPLAY RESET is generated by Q1 inverting $\overline{\text{RCV WORD}}$.

c) VALID WORD Generation

VALID WORD lights the VALID WORD indicator for 15 msec. minimum. The VALID WORD indicator lights at the end of each valid received word, that is, words parity checking correctly. VALID WORD Pin C(3) is generated by NOR GATES IC2A and IC2B. IC2A, IC2B, C3 and R4 combined form an 18 msec. monostable. VALID WORD will be initiated by the output from the AND GATE comprised of CR1, CR2, CR3 and R3 on the falling edge of B GATE MONO Pin H(7) only if both $\overline{\text{ERROR WORD}}$ Pin F(6) and R/T CONTROL Pin S(15) are logic 1.

d) Control Signal Buffers

A GATE Pin N(12) is delayed by R1 and C1, and double inverted by IC1A and IC1D to generate A GATE B Pin X (20). B GATE Pin (13) is delayed by R2 and C2 then double inverted by IC1B and IC1E to generate B GATE B Pin T (16). MASTER CLOCK Pin V(18) is buffered by IC1C and IC1F to generate MASTER CLOCK B Pin W (19), A GATE B and B GATE B are applied to board 9004 and MASTER CLOCK B is applied to board 9010.

6) WORD COUNTER AND DISPLAY CONTROL - BOARD 9006

Refer to Figure 7-11 for schematic information and Fig-6-6 for pertinent waveforms.

The WORD COUNTER AND DISPLAY CONTROL Board performs the following functions:

WORD COUNTER A, B, C, and D Generation - SELECTED STROBE + ERROR STROBE Generation
B GATE MONO PI Generation

a) Generation of WORD COUNTER A, B, C, D

In both receive and transmit WORD COUNTER A, B, C and D are binary representations of the word being received or transmitted. WORD COUNTER A is the least significant bit and WORD COUNTER D is the most significant bit. WORD COUNTER A, B, C and D are the outputs of a 4 stage ripple through counter consisting of FLIP-FLOPS IC3A, IC3B, IC5A and IC5B. Counter states 0 through 15 correspond to receive or transmitted words 1 through 16, respectively. The $\overline{Q}$ outputs of IC3A, IC3B, IC5A and IC5B are inverted by INVERTERS IC1F, IC1E, IC1D and IC1C, respectively, to generate WORD COUNTER A, Pin S(15), B Pin R(14), C Pin U(17) and D Pin T(16).

The counter is clocked by $\overline{\text{B GATE MONO}}$ generated at the trailing edge of every B GATE Pin P(13) by INVERTERS IC1A and IC1B. $\overline{\text{B GATE MONO}}$ is inverted by NOR GATE IC4B to generate B GATE MONO, Pin E (5). The word counter is reset by WORD COUNTER RESET Pin B(2).

b) Generation of SELECTED STROBE + ERROR STROBE

[SELECTED STROBE + ERROR STROBE] is generated by controlling B GATE MONO either at NOR GATE IC4C or NOR GATE IC2B, respectively. B GATE MONO is selected at IC4C either by $\overline{A = B}$ logic 0, DISPLAY WORD SELECT Switch in ALL, logic 1 or WORD COUNTER RESET Pin B(2) logic 1. $\overline{A = B}$ will be effective when A0 = B0, A1 = B1, A2 = B2 and A3 = B3 at COMPARATOR IC6. $\overline{A = B}$ is generated by NOR GATE IC4D inverting the A = B output from IC6. The A inputs are generated by the DISPLAY WORD SELECT Switch S(11) positions 1-16 and the B inputs are the Q outputs from the Word Counter. If either WORD COUNTER RESET or DISPLAY SELECT - ALL Pin C(3) is logic 1 then output of NOR GATE IC4A is logic 0 enabling IC4C regardless of $\overline{A = B}$. WORD COUNTER RESET will go to logic 1 if MASTER CLEAR or RECEIVER CLEAR or INDICATOR TEST is pressed.

ERROR STROBE Pin K(9) will be generated at IC2B when the output of the OR GATE comprised of CR2, CR3 and R5 is logic 0 indicating that $\overline{\text{ERROR WORD}}$ Pin F(6) and the output of NOR GATE IC2A are both logic 0. The output of IC2A will be logic 0 when Pin J(8) is logic 1 indicating the DISPLAY ERROR WORD Switch is ON.

TMTL Pin D(4) and $\overline{\text{[SELECTED STROBE + ERROR STROBE]}}$ from NOR GATE IC2C are applied to the OR GATE comprised of CR5, CR6 and R11. The output is inverted by NOR GATE IC2D to generate [SELECTED STROBE + ERROR STROBE] at Pin H(7). When transmitting TMTL at logic 1 will hold [SELECTED STROBE + ERROR STROBE] to logic 0.

c) Generation of B GATE MONO PI

TMTL modifies B GATE MONO to generate B GATE MONO PI Pin N(12) utilizing CR7 and R12. This prevents the PI from being cycled unless transmitting.

7) INTERFACE I — BOARD 9007

Refer to Figure 7-12 for schematic information and Figure 6-7 for pertinent waveforms.

The INTERFACE I board performs the following functions:

RD E1/E2 and RD E2A Generation -
TONE and CD Generation -

a) Generation of RD E1/E2 and RD E2A

RD, RECEIVE DATA, is present at the output of NOR GATE IC1D and level shifted by Q1, Q2 and Q3, and AMPLIFIER IC2, Q4 and Q5 to generate RD E1/E2 Pin X (20) and RD E2A Pin B (2) respectively. The RD format can either be E1/E2 or E2A depending on position of SYSTEM switch.

A + B GATE Pin J(8) is inverted by NOR GATE IC1A and fed to NOR GATE IC1B. TMT WORD Pin H(7) also goes to IC1B. The output of IC1B is fed to NOR GATE IC1D. COUNTER RESET Pin F(6) is fed to IC1D by way of pull-down R24 and CR12. COUNTER RESET pull down is controlled by E2A/E1/E2. With the SYSTEM switch in E2A, E2A/E1/E2 is at logic 1 allowing COUNTER RESET to operate at IC1D. COUNTER RESET is pulled down by E2A/E1/E2 at logic 0 when SYSTEM E1/E2 is selected.

The data formats of RD E1/E2 and RD E2A can be either E1/E2 or E2A, however the signal levels at RD E1/E2 will always satisfy E1/E2 interface requirements and RD E2A will always satisfy E2A interface requirements.

b) Generation of TONE and CD

TONE is present at the Q output of FLIP-FLOP IC3B and level shifted by Q6, Q7 and Q8 to satisfy E1/E2 interface requirements. TONE transitions on a word to word basis only during transmit.

TONE transitions to logic 1 when COUNT 4 appears at the CK terminal of FLIP-FLOP IC3A only when TMTL Pin K(9) is logic 1, since Q output of IC3A sets IC3B. IC3B is held set until B GATE MONO at the end of each word resets IC3A. TONE will then return to logic 0 one count after B GATE MONO due to MASTER CLOCK Pin V(18) clocking IC3B.

CD (CARRIER DETECT) is present at the junction of diodes CR6 and CR7 and level shifted by AMPLIFIER IC4, Q9 and Q10 to satisfy E2A interface requirements. CR5, CR6, CR7 and R12 control the CD wave shape. With the SYSTEM switch in E1/E2 CD will appear identical to TONE. When E2A is selected CD will be the same as TMTL.

The TONE output is present at Pin Y(21) and the CD output is present at Pin E(5).

8) INTERFACE II — BOARD 9008

Refer to Figure 7-13 for schematic information and Figure 6-8 for pertinent waveforms.

The INTERFACE II board performs the following functions:

R/T CONTROL and CTS Generation -
RCV INFO BITS Generation -
RCV EXT CLK Generation -

a) Generation of R/T CONTROL

R/T CONTROL normally is at logic 0 and will go to logic 1 to indicate data is being received. R/T CONTROL will be logic 1 if $\overline{\text{TMT}}$ ($\overline{\text{TRANSMIT}}$) of $\overline{\text{GR}}$ ($\overline{\text{GROUP REPORT}}$) go to logic 0, 21 ±5 v or RTS (Ready to Send) goes to logic 1, +8 ± 3 v, in E1/E2 or E2A operation, respectively. This 3 input OR function is performed by diodes CR4, CR5, and CR6. Diodes CR1, CR2 and CR3 perform the same OR function to generate RCV LAMP DRIVE when data is being received. The junction of CR4, CR5 and CR6 feeds transistors Q1 and Q2 which in turn drive TIMER IC1. TIMER IC1 is set to integrate for 60 msec to prevent transitions of $\overline{\text{TMT}}$, $\overline{\text{GR}}$ or RTS from transitioning R/T CONTROL except at the end of the received message.

CTS (CLEAR TO SEND) is generated by applying the output of transistor Q2 to TIMER IC2. TIMER IC2 causes CTS to go to logic 1, +8 ±3v, approximately 15 msec after RTS goes to logic 1, if the test set is not transmitting, TMTL, Pin B(2) at logic 0. CTS returns to logic 0 at the same time RTS returns to logic 0. Amplifier IC3, Q3, Q4 and Q5 level shift CTS from 0 to 5 v logic levels to E2A interface levels.

b) Generation of RCV INFO BITS

RCV INFO BITS Pin K(9) is generated by applying SD (SEND DATA) or TD (TRANSMIT DATA) Pin J(8) to transistor Q9 in E1/E2 or E2A, respectively. Q9 level shifts and inverts SD or TD to generate RCV INFO BITS, 0 v to 5 v logic.

c) Generation of RCV EXT CLK

RCV EXT CLK Pin Y(21) is a positive pulse generated by either positive transitions, 0 +.5, -0 v to +14 ±12 v or negative transitions, +14 ±12 v to 0 +.5, -0 v at the RCV EN IN (Receive Enable Input) binding posts. The position of the ENABLE switch determines which transitions will generate RCV EXT CLK, +EXT indicates positive transitions and -EXT indicates negative transitions. In +EXT the input is routed to RCV EN IN (+) Pin V(18) and processed by transistors Q7 & Q8. In -EXT it is routed to RCV EN IN (-) Pin U(17) and processed by transistors Q6, Q7 and Q8.

DTR (DATA TERMINAL READY) Pin X(20) is applied to R43, R44 and CR13 and brought out as DTR LAMP DRIVE Pin W(19) to light the DTR lamp.

9) POWER SUPPLY — BOARD 9009

Refer to Figure 7-14 for schematic information. This circuit board and associated chassis mounted components (shown outside the dashed border) make up the "POWER SUPPLY." All of the appropriate supply levels for the Interface circuitry and logic boards in the BTS and all boards in the PI units are derived from this supply. The operation of this circuit is as follows:

a) The power transformer (T1) steps down the line voltage to 25.2 Vrms (center tapped).

b) The center-tapped secondary feeds —

1) The positive full wave/filtered circuitry comprised of CR1, CR2 and C1 (chassis mounted components). This network in turn supplies a 9.5 volt series regulator circuit which consists of Q1, VR1, R1, R2 and C1. The 9.5 volt supply is used to power the PI UNITS via the rear connector and WORD DISPLAY Board 9010 and Interface I and II Boards 9007 and 9008 in the BTS.

2) The negative full wave zener regulated supply which consists of CR1, CR2, C6, R3, CR3 and C7 and supplies the Interface circuits with (-8V).

3) The positive voltage doubler circuitry consists of C5, CR4, CR5, C8 and regulating components R4 and CR6. +20 v is obtained at the output of this circuit which supplies the Interface circuits.

c) VR2, VR3 and associated components share the +5 volt logic load demand in the BTS.

d) R5 acts as a voltage dropping resistor for the POWER ON Indicator (LED 1).

10) WORD DISPLAY — BOARD 9010

Refer to Figure 7-15 for schematic information. The WORD DISPLAY Board performs the following functions:

Display DISPLAY INFO —
Display Status Indicators —

a) Display DISPLAY INFO

DISPLAY INFO Pin Y(21) is clocked through a 25 bit shift register consisting of 8 BIT SHIFT REGISTERS, IC1, IC2 and IC3 and FLIP-FLOP IC10A. Buffered MASTER CLOCK [MASTER CLOCK B] Pin W(19) clocks the 25 bit shift register. The 24 Q outputs from IC1, IC2 and IC3 are fed to six 4 BIT BISTABLE LATCHES IC4, through IC9. The Q output of IC10A DISPLAY INFO D is fed to FLIP-FLOP IC10B which functions as a latch for bit 25. DISPLAY INFO D Pin X (20) also goes to board 9004, PARITY GENERATOR/ CHECKER, CONTROL in order to check parity when receiving.

The 25 bit latch is clocked by DISPLAY STROBE. Transistors Q1 and Q2 buffer DISPLAY STROBE. DISPLAY STROBE Pin V(18) will transfer the state of 25 bit shift register to the output of the 25 bit latch. Using the $\overline{Q}$ outputs of the latch causes LED 1 through 25 to light when the respective bit position of the 25 bit shift register is logic 1. LED 25 labelled E2A CONT is held reset when SYSTEM E1/E2 is selected by applying logic 0 to Pin Z(22). This reset condition is released when SYSTEM E2A is selected or INDICATOR TEST is pressed. When INDICATOR TEST is pressed DISPLAY INFO at logic 1 causes all 25 indicators to light.

DISPLAY CLEAR Pin L(10) clears the 25 bit shift register making all outputs logic 0. RCV BITS A, B and C at Pins M(11), N(12) and P(13) reflect the state of displayed bits 1, 2, and 3.

b) Display Status Indicators

The WORD DISPLAY Board contains status indicators labelled TMT, DTR, RCV, ERROR WORD and VALID WORD corresponding to LEDS 26 through 30 respectively. Transistors Q3 through Q7 drive LEDS 26 through 30. These indicators will light when their respective inputs, TMTL Pin U(17), DTR LAMP DRIVE Pin T(16), RCV LAMP DRIVE Pin S(15), ERROR WORD Pin A(1) and VALID WORD Pin F(6) are logic 1. All 5 indicators will light as long as INDICATOR TEST is held applying logic 1 to Pin E(5).

Voltage regulators VR1 and VR2 shift the 9.5 V Pin R(14) input to +5VDC.

3-3b. Model 2476 Circuitry

1) INSTRUCTION CONTROL LOGIC I — BOARD 9051

Refer to Figure 7-18 for schematic information and Figure 6-9 for pertinent waveforms. The primary function of the Instruction Control Logic 1 board is to latch in the desired instruction and to reset the latch associated with the previously chosen instruction. This is accomplished by allowing INSTR LATCH CLK, Pin U (17), to clock FLIP-FLOPS IC2A, IC3A, IC3B and IC2B by way of Pin Z (22) whenever an instruction pushbutton is pressed. ALARM REPORT, Pin X (20), GROUP REPORT, Pin K (9), DISPLAY REPORT, Pin J (8), and REMOTE SWITCH, Pin L (10), normally maintain the D terminals of IC2A, IC3A, IC3B and IC2B at logic 0. When an instruction pushbutton is pressed the D terminal of its respective FLIP-FLOP will go to logic 1. This logic 1 will be transferred to the output of the FLIP-FLOP. All other FLIP-FLOPS will go to or remain at logic 0. INSTR LATCH CLK (100 Hz) is generated by INVERTERS IC1A, IC1B and associated circuitry. The outputs from IC2A, IC3A, IC3B and IC2B designated AR, GR, DR and RS respectively are applied to Pins W (19), D (4), E (5) and F (6) respectively. AR, GR, DR and RS are fed to word register boards 9052, 9053 and 9054 to control shift register loading depending on the chosen instruction. AR, GR, DR and RS are inverted by INVERTERS IC1C, IC1D, IC1E and IC1F respectively to supply drive to the instruction indicators LED1, LED2,

LED3 and LED4 by way of Pins T (16), P (13), H (7) and N (12) respectively. $\overline{DR}$ is available at Pin R (14) and $\overline{RS}$ is available at Pin S (15). INDICATOR TEST, Pin V (18), tests the instruction indicators by setting the outputs of IC2A, IC3A, IC3B and IC2B to logic 1. MASTER CLEAR, Pin Y (21), clears the instruction latches by resetting the outputs of IC2A, IC3A, IC3B and IC2B to logic 0. INSTR LATCH CLK is applied to QUICK REPLY and REMOTE CALL UP instruction switches and Pin Z (22) is fed to Board 9057, Pin D (4), to interlock two additional instruction latches on Board 9057 with the latches on this board.

2) WORD 2 SHIFT REGISTER (BITS 1-17) — BOARD 9052

Refer to Figures 7-19 for schematic information and Figure 6-10 for pertinent waveforms. The primary function of the Word 2 Shift Register Board is to parallel load and serial shift the data content of Word 2 whenever two word messages are generated. The output from this board WORD 2 PIN B (2), is only utilized when either DISPLAY REPORT or REMOTE SWITCH instructions are initiated. Parallel loading and serial shifting is accomplished using two 8 BIT SHIFT REGISTERS IC1 and IC2. The SI input to IC1 is used to control Bit 17. Since Bit 1 of Word 2 is always logic 1 Pin 1 of IC2 is connected to +5V. Since Bits 8, 10, 11, 15, 16 and 17 are always logic 0 Pin 7 of IC2 and Pins 15, 14, 6, 7 and 11 of IC1 are connected to ground. Bits 2-7, 13 and 14 are determined by two quad AND OR SELECT GATES IC3 and IC4. When the DISPLAY REPORT instruction is initiated DR Pin E (5) goes to logic 1. This gate select control level will allow transfer of all "A" data present to IC1 and IC2. When the REMOTE SWITCH instruction is initiated, RS, Pin F(6), goes to logic 1. This in turn allows transfer of all "B" data present to IC1 and IC2. Bits 9 and 12 are directly controlled by DR and RS respectively. REMOTE SWITCH switches S6B and S6C supply the "B" inputs to IC3 and IC4. DISPLAY switch S5 supplies two "A" inputs to IC3. When DATA PAR/SER Pin X (20) is a logic 1 all data at the parallel inputs to IC1 and IC2 is jammed into the shift registers regardless of the DATA CLK Pin Y(21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of DATA CLK.

3) WORD 1 SHIFT REGISTER (BITS 9-17) — BOARD 9053

Refer to Figure 7-20 for schematic information and Figure 6-10 for pertinent waveforms. The primary function of the Word 1 Shift Register (Bits 9-17) Board is to parallel load and serial shift the data content of Bits 9-17 of Word 1. The output from this board WORD 1, (9-17), Pin K (9) is applied to Board 9054 where Bits 1-8 of Word 1 are parallel loaded and serial shifted. Parallel loading and serial shifting is accomplished using an 8 BIT SHIFT REGISTER IC2. The SI input to IC2 is used to control Bit 17. Since Bits 10 and 11 are always logic 0 Pins 14 and 15 of IC2 are connected to ground. Bit 9 is controlled by the STATION switch at Pin J (8). Bits 12 and 13 are controlled by NOR GATES IC1A, IC1B and IC1C. When QUICK REPLY is selected [RCU + QR] Pin C (3) goes to logic 1 and $\overline{QR}$ to S10 and S11 goes to logic 0 making the output of IC1A logic 0 permitting Bit 12, the output of IC1C, to be controlled by the DI Switch (S11) Pin H (7). IC1B is also enabled thereby allowing the TE-NE Switch (S10) to contol Bit 13. If any of the other instruction switches are pressed Bits 12 and 13 will be held to logic 0. Bits 14, 15, 16 and 17 are controlled by quad AND OR SELECT GATES IC4 and IC5 and NOR GATES IC3A, IC3B, IC3C and IC1D. When ALARM REPORT is selected AR Pin W (19) goes to logic 1 selecting the "A" inputs to IC4, logic 0 for Bits 14, 15, 16 and 17. IC3A, IC3B, IC3C and IC1D combine to form a 4 input OR function such that the output of IC1D will go to logic 1 upon selection of either REMOTE SWITCH, GROUP REPORT, DISPLAY REPORT, [REMOTE CALL UP or QUICK REPLY] instructions causing RS Pin F (6), GR Pin D (4), DR Pin E (5) or [RCU + QR] Pin C (3) to go to logic 1 respectively. The output of IC1D at logic 1 selects the "B" inputs to IC4 for Bits 14, 15, 16 and 17. The "B" inputs to IC4 are the selected output from IC5. The output from IC5 will be the "B" input when RS goes to logic 1. If either GR, DR or [RCU + QR] goes to logic 1 then the "A" inputs to IC5 will be selected. The REMOTE SWITCH switch (S6A) provides the B inputs to IC5 and GRP/1/0 Switch (S7) provides the A inputs. The A inputs to IC5 are held to logic 0's when QUICK REPLY is selected since $\overline{QR}$ + 5V is held to 0 volts. When DATA PAR/SER Pin X (20) is a logic 1 all data at the parallel inputs to IC2 is jammed into the register regardless of the DATA CLK Pin Y (21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edges of DATA CLK.

4) WORD 1 SHIFT REGISTER (BITS 1-8) — BOARD 9054

Refer to Figure 7-21 for schematic information and Figure 6-10 for pertinent waveforms. The primary function of the Word 1 Shift Register (Bits 1-8) Board is to parallel load and serial shift the data content of Bits 1-8 of WORD 1 Pin N (12). Parallel loading and serial shifting is accomplished using an 8 BIT SHIFT REGISTER IC2. Bit 1 controlled by [RCU + QR] Pin C (3) will be logic 1 when [RCU + QR] is logic 1. Bit 2 is controlled by NOR GATES IC1A, IC1B, IC1C and IC1D. If either DISPLAY REPORT, REMOTE SWITCH or GROUP REPORT are chosen DR Pin E (5), RS Pin F (6) or GR Pin D (4) will go to logic 1. This logic 1 will appear at the output IC1D to control Bit 2. Bit 3 is controlled by the output of IC1B which will be logic 1 if either DISPLAY REPORT or REMOTE SWITCH instructions are chosen. Bits 4-8 are controlled by STATION Switches S8A and S8B only if QUICK REPLY is not chosen. If QUICK REPLY is selected then $\overline{QR}$ + 5V will be 0 volts and Bits 4-8 will be logic 0. WORD 1 (9-17) Pin K (9) is applied to the SI input of IC2 to be shifted through IC2 such that WORD 1 Pin N (12) contains all 17 bits. When DATA PAR/SER Pin X

(20) is a logic 1 all data present at the parallel inputs to IC2 is jammed into the register regardless of the DATA CLK Pin Y (21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of the DATA CLK.

5) TRANSMIT WORD CONTROL — BOARD 9055

Refer to Figure 7-22 for schematic information and Figure 6-11 for pertinent waveforms. The Transmit Word Control Board performs the following functions:

Generates COUNTER RESET
Generates DATA PAR/SER and DATA CLK

a) COUNTER RESET GENERATION

COUNTER RESET Pin T (16) is generated by FLIP-FLOP IC4A, COMPARATOR IC3 and NAND GATES IC1A, IC1B, IC2A and IC2B. The required message length is determined by the selected instruction. When DISPLAY REPORT or REMOTE SWITCH is selected $\overline{DR}$ Pin P (13) or $\overline{RS}$ Pin N (12) goes to logic 0 making B0 logic 1 indicating a two word message. When REMOTE CALL UP is selected $\overline{RCU}$ Pin H (7) goes to logic 0 making B0, B1, B2 and B3 logic 1 indicating a 16 word message. All other instructions make B0-B3 logic 0 indicating a 1 word message. COUNTER RESET is generated by comparing the required message length with the accumulated word count WORD COUNTER A, B, C, and D Pins E (5), C (3), D (4) and F (6) respectively. When an equality exists the output of IC3 goes to logic 1 enabling IC2B to pass B GATE PI Pin B (2) delayed by R2 and C1. The output of IC2B clocks IC4A at the falling edge of B GATE PI. One clock count later the positive edge of MASTER CLOCK Pin S (15) differentiated by C3 and R4 resets IC4A making COUNTER RESET one clock count wide following the last B GATE PI.

b) DATA PAR/SER AND DATA CLK GENERATION

DATA PAR/SER is actually a reclocked and inverted A GATE. FLIP-FLOP IC4B performs this function with A GATE Pin R (14) applied to the D terminal and the MASTER CLOCK Pin S (15) delayed by R5 and C4 applied to the CK terminal. The $\overline{Q}$ output of IC4B is then delayed by R6 and C5 to generate DATA PAR/SER, Pin X (20).

DATA CLK, Pin Y (21) signal is generated by applying the MASTER CLOCK and the Q output of IC4B to NAND GATE IC2C whose output is then inverted by IC2D.

6) TRANSMIT WORD SELECTOR — BOARD 9056

Refer to Figure 7-23 for schematic information and Figure 6-12 for pertinent waveforms.

The Transmit Word Selector Board performs the following functions:

Generate +5V
Generate $\overline{QR}$ +5V
Generate TMT INFO BITS

a) +5V GENERATION

Regulated +5 Volts Pin M(11) for all plug in boards in this PI is generated by VOLTAGE REGULATOR VR1. The input to VR1 is +9.5V Pin Y (21).

b) $\overline{QR}$ +5V GENERATION

$\overline{QR}$ +5V Pin K(9) provides an inhibit of the Station (a1/a2) and GRP/1/0 (b) thumbwheel data when the QUICK REPLY Instruction is initiated by turning off the +5V to the respective switches. $\overline{QR}$ Pin L(10) applied to Q1, Q2 and their associated components perform this function.

c) TMT INFO BITS GENERATION

TMT INFO BITS Pin V(18) is generated by Quad BI LATERAL SWITCH IC1, NOR GATES IC3A and IC3B and FLIP-FLOP IC2A. WORD 1 Pin N(12), WORD 2 Pin P(13) and WORD 1+Pin S(15) are applied to the D, A and B inputs of IC1. The output of IC1 will be the input whose control is at logic 1. WORD 1 CONTROL is generated by IC3A from WORD COUNTER A, B, C and D at Pins E(5), C(3), D(4) and F(6) respectively. WORD 1 CONTROL will go to logic 1 only when the Word Counter is in its reset state all zeros, thereby first selecting WORD 1. When transmitting a two word message WORD 1+ CONTROL Pin T(16) and RCU Pin H(7) will remain at logic 0. WORD 2 will be selected after WORD 1 since the output of IC3B goes to logic 1 when WORD 1 CONTROL goes to logic 0. Transmission of a 16 word message only occurs when REMOTE CALL UP is initiated. In this case RCU at logic 1 holds the output of IC3B to logic 0 allowing WORD 1+ CONTROL Pin T(16) to select WORD 1+ for transmission. The output from IC1 is reclocked by MASTER CLOCK only when "A" GATE is logic 1 at IC2A to insert Bit 0 or the sync bit. "A" GATE Pin R(14) is inverted by Q3 to supply a reset to IC2A. The output from IC2A is TMT INFO BITS.

7) INSTRUCTION CONTROL LOGIC II — BOARD 9057

Refer to Figure 7-24 for schematic information and Figure 6-13 for pertinent waveforms.

The Instruction Control Logic II Board performs the following functions:

Instruction Latching
Generates WORD 1+

a) INSTRUCTION LATCHING

QUICK REPLY and REMOTE CALL UP Instruction Switches (S12 and S13) Pins K(9) and F(6) are latched by FLIP-FLOPS IC1A and IC1B respectively. IC1A and IC1B are interlocked with the 4 instruction latches on Board 9051 such that only one instruction is initiated at one time. INSTR LATCH CLK clocks IC1A and IC1B by way of Pin D(4).

When QUICK REPLY is selected the Q output of IC1A goes to logic 1 causing [RCU + QR] Pin N(12) to go to logic 1 and $\overline{QR}$ Pin L(10) to logic 0. When REMOTE CALL UP is selected the Q terminal of IC1B goes to

logic 1 causing [RCU + QR] and RCU Pin J(8) to go to logic 1 and $\overline{RCU}$ Pin U(17) to logic 0. NOR GATE IC2A is also enabled allowing WORD 1 CONTROL Pin V(18) to be inverted to generate WORD 1+ CONTROL Pin T (16). Q1 and Q2 act as inverter buffers to turn on the respective instruction indicators at Pins B(2) and C(3). [RCU + QR] is generated by OR function comprised of CR1, CR2 and R6. INDICATOR TEST PIN H(7) and MASTER CLEAR Pin E(5) test and clear the instruction indicators respectively.

b) WORD 1+ GENERATION

WORD 1+ Pin S(15) is the information for words 2, 3,.... 16 when REMOTE CALL UP is selected. WORD 1+ is generated by FLIP-FLOPS IC3A, IC4A and IC4B, NOR GATES IC2B, IC2C and IC2D, OR function comprised of CR5, CR7 and R13, and AND function comprised by CR4, CR6 and R12. DATA CLK Pin X(20) delayed by R8 and C1 clocks IC3A which is set up to divide by 2 to generate DATA CLK ÷2 Pin Y(21) and $\overline{\text{DATA CLK ÷2}}$ Pin Z(22). DATA CLK delayed by R9 and C2 also clocks IC4A. Q output of IC4 clocks IC4B whose $\overline{Q}$ output is used such that the Q output of IC4A remains at logic 1 for Bit 1. IC3A, IC4A and IC4B are reset by "A" GATE Pin W(19) differentiated by C3, R10, R11 and CR3. BIT 1 applied to IC2C by way of CR7 satisfies the requirement that Bit 1 of WORD 1+ words be logic 1. DATA CLK ÷2 and $\overline{\text{DATA CLK ÷2}}$ are fed to DATA PATTERN Switch (S14) to be selected in positions B and A respectively. DATA PATTERN SWITCH Pin R(14) is applied to IC2B and IC2C by way of CR6. WORD COUNTER A is also applied to IC2B and IC2C by way of CR6. WORD COUNTER A is also applied to IC2B and IC2C by way of CR4 to satisfy the data "checkerboard" requirement for Bits 2-17 of WORD 1+ words. The data "checkerboard" requires that in position A all even number words contain logic 1 in even numbered bit positions and all odd number words contain logic 1 in odd numbered bits positions and a reversed pattern in position B.

3-3c. Model 2475 Circuitry

1) INSTRUCTION CONTROL LOGIC 1 — BOARD 9051

Refer to Figure 7-27 for schematic information and Figure 6-14 for pertinent waveforms.

The primary function of the Instruction Control Logic 1 board is to latch in the desired instruction and to reset the latch associated with the previously chosen instruction. This is accomplished by allowing INSTR LATCH CLK Pin U (17) to clock FLIP-FLOPS IC2A, IC3A, IC3B and IC2B by way of Pin Z (22) whenever an instruction pushbutton is pressed. ALARM REPORT Pin X (20), GROUP REPORT Pin K (9), DISPLAY REPORT Pin J (8) and REMOTE SWITCH Pin L (10) normally maintain the D terminals of IC2A, IC3A, IC3B and IC2B at logic 0. When an instruction pushbutton is pressed the D terminal of its respective FLIP-FLOP will go to logic 1. This one will be transferred to the output of the FLIP-FLOP. All other FLIP-FLOPS will go to or remain at logic 0. INSTR LATCH CLK (100 Hz) is generated by INVERTERS IC1A, IC1B and associated circuitry. The outputs from IC2A, IC3A, IC3B and IC2B designated AR, GR, DR and RS respectively are applied to Pins W (19), D (4),E (5) and F (6) respectively. AR, GR, DR and RS are fed to word register boards 9052, 9053 and 9054 to control shift register loading depending on the chosen instruction. AR, GR, DR and RS are inverted by INVERTERS IC1C, IC1D, IC1E and IC1F respectively to supply drive to the instruction indicators LED1, LED2, LED3 and LED4 by way of Pins T (16), P (13), H (7), and N (12) respectively. $\overline{DR}$ is available at Pin R (14) and $\overline{RS}$ is available at Pin S (15). INDICATOR TEST Pin V (18) tests the instruction indicators by setting the outputs of IC2A, IC3A, IC3B and IC2B to logic 1. MASTER CLEAR Pin Y (21) clears the instruction latches by resetting the outputs of IC2A, IC3A, IC3B and IC2B to logic 0.

2) WORD 2 SHIFT REGISTER (BITS 1-17) — BOARD 9052

Refer to Figure 7-28 for schematic information and Figure 6-15 for pertinent waveforms.

The primary function of the Word 2 Shift Register Board is to parallel load and serial shift the data content of Word 2 whenever two word messages are generated. The output from this board WORD 2 Pin B(2) is only utilized when either DISPLAY REPORT or REMOTE SWITCH instructions are initiated. Parallel loading and serial shifting is accomplished using two 8 BIT SHIFT REGISTERS IC1 and IC2. The SI input to IC1 is used to control Bit 17. Since Bit 1 of Word 2 is always logic 1 Pin 1 of IC2 is connected to +5V. Since Bits 8, 10, 11,15, 16 and 17 are always logic 0 Pin 7 of IC2 and Pins 15, 14, 6, 7, and 11 of IC1 are connected to ground. Bits 2-7, 13 and 14 are determined by two quad AND OR SELECT GATES IC3 and IC4. When the DISPLAY REPORT instruction is initiated DR Pin E (5) goes to logic 1. This gate select control level will allow transfer of all "A" data present to IC1 and IC2. When the REMOTE SWITCH instruction is initiated RS Pin F (6) goes to logic 1. This in turn allows transfer of all "B" data present to IC1 and IC2. Bits 9 and 12 are directly controlled by DR and RS respectively. REMOTE SWITCH switches S6B and S6C supply the "B" inputs to IC3 and IC4. DISPLAY switch S5 supplies two "A" inputs to IC3. When DATA PAR/SER Pin X(20) is a logic 1 all data at the parallel inputs to IC1 and IC2 is jammed into the shift registers regardless of the DATA CLK, Pin Y (21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of DATA CLK.

3) WORD 1 SHIFT REGISTER (BITS 9-17) —BOARD 9053

Refer to Figure 7-29 for schematic information and Figure 6-15 for pertinent waveforms.

The primary function of the Word 1 Shift Register (Bits 9-17) Board is to parallel load and serial shift the data content of Bits 9-17 of Word 1. The output from this board WORD 1 (9-17) Pin K (9) is applied to Board 9054 when Bits 1-8 of Word 1 are parallel loaded and serial shifted. Parallel loading and serial shifting is accomplished using an 8 BIT SHIFT REGISTER IC2. The SI input to IC2 is used to control Bit 17. Since Bits 10 and 11 are always logic 0 Pins 14 and 15 of IC2 are connected to ground. Bit 9 is controlled by the STATION Switch at Pin J (8). Bits 12 and 13 are held to logic 0 by NOR GATES IC1B and IC1C, since Pins B (2) and H (7) are always at logic 1. Bits 14, 15, 16 and 17 are controlled by quad AND OR SELECT GATES IC4 and IC5 and NOR GATES IC3A, IC3B, IC3C and IC1D. When ALARM REPORT is selected AR Pin W (19) goes to logic 1 selecting the "A" inputs to IC4 logic 0 for Bits 14, 15, 16 and 17. IC3A, IC3B, IC3C and IC1D combine to form a 3 input OR function such that the output of IC1D will go to logic 1 upon selection of either REMOTE SWITCH, GROUP REPORT or DISPLAY REPORT instructions causing RS Pin F (6), GR Pin D (4) or DR Pin E (5) to go to logic 1 respectively. The output of IC1D at logic 1 selects the "B" inputs to IC4 for Bits 14, 15, 16 and 17. The "B" inputs to IC4 are the selected output from IC5. The output from IC5 will be the "B" inputs when RS goes to logic 1. If either GR or DR goes to logic 1 then the "A" inputs to IC5 will be selected. The REMOTE SWITCH Switch (S6A) provides the B inputs to IC5 and GRP/1/0 Switch (S7) provides the A inputs. When DATA PAR/SER Pin X (20) is a logic 1 all data at the parallel inputs to IC2 is jammed into the register regardless of the DATA CLK Pin Y (21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of DATA CLK.

4) WORD 1 SHIFT REGISTER (BITS 1-8) - BOARD 9054

Refer to Figure 7-30 for schematic information and Figure 6-15 for pertinent waveforms.

The primary function of the Word 1 Shift Register (Bits 1-8) Board is to parallel load and serial shift the data content of Bits 1-8 of WORD 1 Pin N (12). Parallel loading and serial shifting is accomplished using an 8 BIT SHIFT REGISTER IC2. Bit 1 is held to logic 0 since Pin C (3) is held grounded. Bit 2 is controlled by NOR GATES IC1A, IC1B, IC1C and IC1D. If either DISPLAY REPORT, REMOTE SWITCH or GROUP REPORT are chosen DR Pin E (5), RS Pin F (6) or GR Pin D (4) will go to logic 1. This logic 1 will appear at the output IC1D to control Bit 2. Bit 3 is controlled by the output of IC1B which will be logic 1 if either DISPLAY REPORT or REMOTE SWITCH instructions are chosen. Bits 4-8 are controlled by STATION Switches S8A and S8B. WORD 1 (9-17) Pin K (9) is applied to the SI input of IC2 to be shifted through IC2 such that WORD 1 Pin N (12) contains all 17 bits. When DATA PAR/SER Pin X (20) is a logic 1 all data present at the parallel inputs to IC2 is jammed into the register regardless of the DATA CLK Pin Y (21). When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of the DATA CLK.

5) TRANSMIT WORD CONTROL — BOARD 9055

Refer to Figure 7-31 for schematic information and Figure 6-16 for pertinent waveforms.

The Transmit Word Control Board performs the following functions:

Generates COUNTER RESET
Generates DATA PAR/SER and DATA CLK

a) COUNTER RESET GENERATION

1) COUNTER RESET Pin T (16) is generated by FLIP-FLOP IC4A, COMPARATOR IC3 and NAND GATES IC1A, IC1B, IC2A and IC2B. The required message length is determined by the selected instruction. When DISPLAY REPORT or REMOTE SWITCH is selected $\overline{DR}$ Pin P (13) or $\overline{RS}$ Pin N (12) goes to logic 0 making B0 logic 1 indicating a two word message. All other instructions make B0-B3 logic 0 indicating a 1 word message. COUNTER RESET is generated by comparing the required message length with the accumulated word count WORD COUNTER A, B, C, and D Pins E(5), C (3), D (4) and F (6) respectively. When an equality exists the output of IC3 goes to logic 1 enabling IC2B to pass B GATE PI Pin B (2) delayed by R2 and C1. The output of IC2B clocks IC4A at the falling edge of B GATE PI. One clock count later the positive edge of MASTER CLOCK Pin S (15) differentiated by C3 and R4 resets IC4A making COUNTER RESET one clock count wide following the last B GATE PI.

b) DATA PAR/SER AND DATA CLK GENERATIONS

DATA PAR/SER is actually a reclocked and inverted A GATE. FLIP-FLOP IC4B performs this function with A GATE Pin R (14) applied to the D terminal and the MASTER CLOCK Pin S (15) delayed by R5 and C4 applied to the CK terminal. The $\overline{Q}$ output of IC4B is then delayed by R6 and C5 to generate DATA PAR/SER, Pin X (20).

DATA CLK Pin Y (21) signal is generated by applying the MASTER CLOCK and the Q output of IC4B to NAND GATE IC2C whose output is then inverted by IC2D.

6) TRANSMIT WORD SELECTOR — BOARD 9056

Refer to Figure 7-32 for schematic information and Figure 6-16 for pertinent waveforms.

The Transmit Word Selector Board performs the following functions:

Generate +5V
Generate S/G +5V
Generate TMT INFO BITS

a) +5V GENERATION

Regulated +5 Volts Pin M (11) for all plug in boards in this PI is generated by VOLTAGE REGULATOR VR1. The input to VR1 is +9.5V Pin Y (21).

b) S/G +5V GENERATION

S/G +5V Pin K (9) provides +5V to the Station (a1/a2) and GRP/1/0 (b) thumbwheel switches. Q1, Q2 and their associated components perform this function.

c) TMT INFO BITS GENERATION

TMT INFO BITS Pin V(18) is generated by quad BILATERAL SWITCH IC1, NOR GATES IC3A and IC3B and FLIP-FLOP IC2A. WORD 1 Pin N (12) and WORD 2 Pin P (13) are applied to the D and A inputs of IC1. The output of IC1 will be the input whose control is at logic 1. WORD 1 CONTROL is generated by IC3A from WORD COUNTER A, B, C and D at Pins E (5), C (3), D (4) and F (6) respectively. WORD 1 CONTROL will go to logic 1 only when the Word Counter is in its reset state, all zeros, thereby first selecting WORD 1. When transmitting a two word message WORD 2 will be selected after WORD 1 since the output of IC3B goes to logic 1 when WORD 1 CONTROL goes to logic 0. The output from IC1 is reclocked by MASTER CLOCK only when "A" GATE is logic 1 at IC2A to insert Bit 0 or the sync bit. "A" GATE Pin R (14) is inverted by Q3 to supply a reset to IC2A. The output from IC2A is TMT INFO BITS.

3-3d. Model 2477 Circuitry

1) WORD 1 AND 2 REGISTER — BOARD 9071

Refer to Figure 7-35 for schematic information and Figure 6-17 for pertinent waveforms.

The primary function of the Word 1 and 2 Register Board is to parallel load and serial shift the data content of Word 1 and Word 2. Word 1 and Word 2 data comes from the respective front panel toggle switches. The outputs from this board are WORD 1 at Pins 1/K and 1/9 and WORD 2 at Pins 1/P and 1/13. Parallel loading and serial shifting is accomplished using two 16 bit shift registers consisting of four (4) 8 BIT SHIFT REGISTERS, IC 3 and IC4 for Word 1 and IC1 and IC2 for Word 2. The SI inputs to IC3 and IC1 are used to control Bit 17 of Word 1 and Word 2 respectively. Bits 1-17 of each word are controlled by Switches 1-17 for each word. When DATA PAR/SER Pins 2/U and 2/17 is a logic 1 all data at the parallel inputs to IC1, IC2, IC3 and IC4 is jammed into the shift registers regardless of the DATA CLK Pins 2/X and 2/20. When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of DATA CLK.

2) WORD 3 AND 4 REGISTER — BOARD 9071

Refer to Figure 7-36 for schematic information and Figure 6-17 for pertinent waveforms.

The primary function of the Word 3 and Word 4 Register Board is to parallel load and serial shift the data content of Word 3 and Word 4. Word 3 and Word 4 data comes from the respective front panel toggle switches. The outputs from this board are WORD 3 at Pins 1/K and 1/9 and WORD 4 at Pins 1/P and 1/13. Parallel loading and serial shifting is accomplished using two 16 bit shift registers consisting of four (4) 8 BIT SHIFT REGISTERS, IC3 and IC4 for Word 3 and IC1, IC2 for Word 4. The SI inputs to IC3 and IC1 are used to control Bit 17 of Word 3 and Word 4 respectively. Bit 1-17 of each word are controlled by Switches 1-17 for each word. When DATA PAR/SER pins 2/U and 2/17 is a logic 1 all data at the parallel inputs to IC1, IC2, IC3 and IC4 is jammed into the shift registers regardless of the DATA CLK Pins 2/X and 2/20. When DATA PAR/SER is at logic 0 data is shifted serially synchronous with the positive edge of DATA CLK.

3) TRANSMIT WORD SELECTOR AND CONTROL — BOARD 9073

Refer to Figure 7-37 for schematic information and Figure 6-18 for pertinent waveforms.

The Transmit Word Selector and Control Board performs the following functions:

Generate DATA PAR/SER and DATA CLK
Generate TMT INFO BITS
Generate COUNTER RESET

a) GENERATION OF DATA PAR/SER AND DATA CLK

The DATA PAR/SER signal is actually a reclocked and inverted A GATE. FLIP-FLOP IC12B performs this function with A GATE Pin 2/Y (21) applied to the D terminal and the MASTER CLOCK Pin 2/X (20) delayed by R7 and C6 applied to the CK terminal. The $\overline{Q}$ output of IC12B is then delayed by R10 and C8 to generate DATA PAR/SER Pin 2/V (18).

DATA CLK Pin 2/U (17) is generated by applying the MASTER CLOCK and the Q output of IC12B to NAND GATE IC11C whose output is then inverted by IC11D.

b) TMT INFO BITS GENERATION

RCU SWITCH "OFF" — PIN 1/B (2) LOGIC 1

When the RCU Switch is in the OFF position NAND GATE IC5C is enabled and NAND GATE IC5B is inhibited by way of NOR GATE IC6C and NAND GATE IC7A is inhibited by way of NOR GATE IC6B. Initially the Word Counter in the Basic Test Set lies in reset state zero making Word Counter A, B, C and D Pins 1/Y (21) 1/X (20), 1/W (19) and 1/Z (22) logic 0, and the output of NOR GATE IC1A logic 1. This logic 1 is then gated by

NAND GATES IC5C and IC5D making the output of IC5D WORD 1 CONTROL, logic 1. WORD 1 CONTROL at logic 1 is applied to "A" control of QUAD BI-LATERAL SWITCH IC13 thereby transmitting Word 1 since the output of the Word 1 register is applied to the "A" input. Words 2, 3 and 4 are then selected by a three stage ring counter consisting of FLIP-FLOPS IC2A, IC2B and IC3A. This ring counter is synchronously clocked by B GATE MONO PI Pin 2/M (11) a 50-100 usec wide positive pulse occurring at the end of every B GATE during transmit. The logic 1 present at the D terminal of FLIP-FLOP IC2A is then transferred to the Q terminal, WORD 2 CONTROL, at the end of Word 1. The Word Counter is also advanced at the end of Word 1 causing the output of IC5D and the D terminal of IC2A to return to logic 0.

WORD 2 CONTROL is applied to the "C" control of IC13. Since the Word 2 register output is applied to the "C" input Word 2 is now selected for transmission. Words 3 and 4 are selected in a likewise fashion; that is by transferring the logic 1 control from IC2A to IC2B (WORD 3 CONTROL) and then to IC3A (WORD 4 CONTROL) at the end of Words 2 and 3 respectively.

During the selection of Word 4 the logic 1 present at the Q terminal of IC3A is applied by way of CR3 and R2 to the D terminal of IC2A thereby selecting Word 2 after Word 4. This generates 16 word messages having the word sequence 1, 2, 3, 4, 2, 3, 4, 2, 3, 4, 2, 3, 4, 2,3, 4.

The output of IC13 is applied to the D terminal of IC3B and the MASTER CLOCK Pin 2/X (20) to the CK terminal. This provides a 1 bit delay thereby making Bit 0 of all words a logic 0. The A GATE inverted by NOR GATE IC6D and applied to the R terminal of IC3B permits clocking only during the A GATE interval and insures Bit 0 will be at logic 0. The Q output of IC3B is TMT INFO BITS Pin 1/H (7).

RCU SWITCH "ON" — PIN 1/B (2) LOGIC 0

With the RCU Switch in the ON position two messages can be transmitted either a 1 word message consisting of Word 1 or a 3 word message consisting of Words 2, 3, and 4. Bits 1, 2 and 3 of the displayed word determines the transmitted reply message. If RCU Bits A, B and C Pins 1/D(4), 1/E(5) and 1/F(6) are logic 1's corresponding to displayed bits 1, 2, and 3 being log ic 0's then the 1 word message is sent. If RCU Bits A, B, and C are logic 1, 0 and 1, respectively, corresponding to displayed bits 1, 2 and 3 being 0, 1, 0 respectively, then the 3 word message is sent. All other combinations will inhibit replying the making TMT INHIBIT Pin 1/C(3) at the output of NOR GATE IC6A a logic 1. The one word message is controlled by the presence of RCU, A, B and C, logic 1's, at the input of NAND GATE IC4C. The output of IC5D, logic 1 causes Word 1 to be transmitted if the Word Counter is at state zero. The output of IC5D can never be logic 1 if the RCU switch is ON and RCU Bits A, B and C are not logic 1.

The three word message is controlled by the presence of RCU Bits A, B and C being logic 1,0,1 respectively. NAND GATE IC4A inverts RCU Bit B such that all inputs to NAND GATE IC4B are logic 1. The logic 0 output of IC4B and RCU switch being ON cause the output of NOR GATE IC6B to be logic 1. This enables NAND GATE IC7A such that transitions of the word counter to state 0 at the end of the received message set FLIP-FLOP IC2A by way of IC1A, IC7A, IC7B, C2 and R3. By setting the Q terminal of IC2A to logic 1 the first word to be transmitted will be Word 2. Word 3 and Word 4 will follow as has been previously described.

c) GENERATION OF COUNTER RESET

COUNTER RESET is a positive pulse, 1 bit wide, generated at the trailing edge of the last transmitted word for the purpose of resetting the Word Select Ring Counter IC2A, IC2B and IC3A in the PI and the word counter in the Basic Test Set.

Generation of COUNTER RESET depends on comparator IC10 determining an equality between the word counter inputs A0, A1, A2 and A3 and inputs B0, B1, B2 and B3. The B inputs are determined by either the MESSAGE LENGTH Switch Pins 2/F (6), 2/H (7), 2/J (8) and 2/L (10) if the RCU switch is OFF or displayed bits 1, 2, 3, that is RCU Bits A, B, C, if the RCU switch is ON. The B inputs are a digital code of the desired message length minus one. This is true because word counter state zero corresponds to transmitted Word 1. NAND GATES IC7C, IC8A, IC8B, IC8C, IC8D and IC9A, IC9B and IC7D determine the state of the B0-B3 inputs namely [0,0,0,0], [1,0,0,0], [0,1,0,0], [1,1,0,0], or [1,1,1,1] for 1, 2, 3, 4 or 16 word messages respectively. When IC10 detects an equality NAND GATE IC11A is permitted to pass a B GATE MONO PI pulse which is delayed by R6 and C4 and then inverted by NAND GATE IC11B and applied to FLIP-FLOP IC12A. One clock count later MASTER CLOCK differentiated by C5 and R9 resets IC12A. The output of IC12A is COUNTER RESET Pin 2/T (16). The COUNTER RESET and MASTER CLEAR Pin 1/T (16) are then combined by CR6, CR7 and R8 to generate a reset for the word select ring counter.

4) CONNECTOR BOARD — BOARD 9074

Refer to Figure 7-37 for schematic information.

The Connector Board performs the following functions:

Generates +5V
Control Word Indicators

a) +5V GENERATION

Regulated +5V for all plug-in boards in this PI is generated by VOLTAGE REGULATOR VR1. The input to VR1 is +9.5V.

b) WORD INDICATOR CONTROL

The Word Indicators LED1, LED2, LED3 and LED4 are controlled by the WORD 1 CONTROL, WORD 2 CONTROL, WORD 3 CONTROL and WORD 4 CONTROL, respectively. These indicators will light when the respective word is transmitted. Transistor Q2, when turned on, applies +5V to the indicators. Transistor Q2 will be turned on either by signal $\overline{\text{TMTL}}$ being a logic 0 or by transistor Q1 being turned on by applying INDICATOR TEST at logic 1. The indicator circuits will be complete upon turn on of the respective transistors Q3, Q4, Q5 or Q6 by the word control signals from board 9073. INDICATOR TEST, when a logic 1, will turn on Q3, Q4, Q5 and Q6, thereby lighting all the lamps.

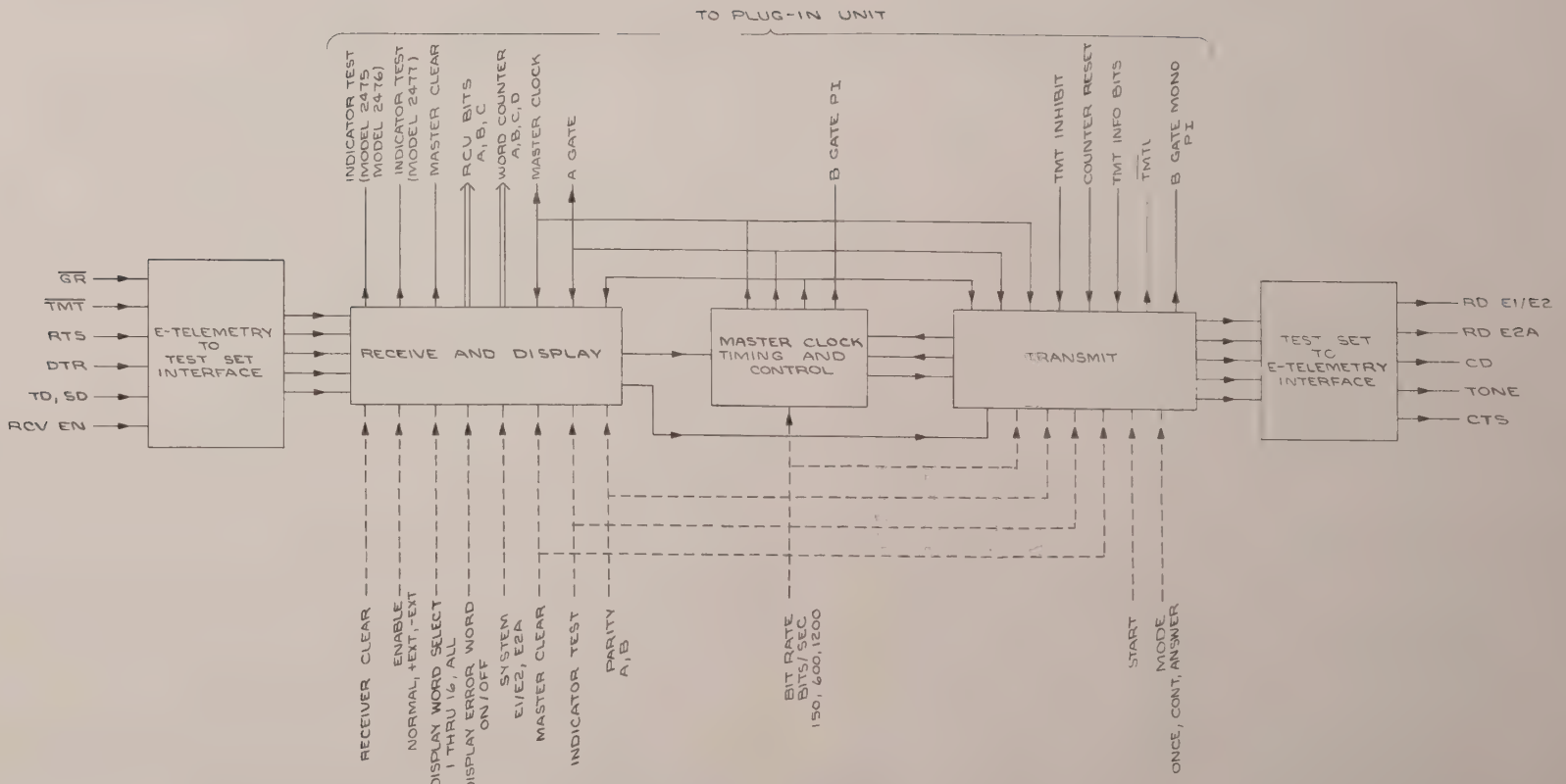


FIGURE 3-1
SIMPLIFIED BLOCK DIAGRAM
MODEL 2474

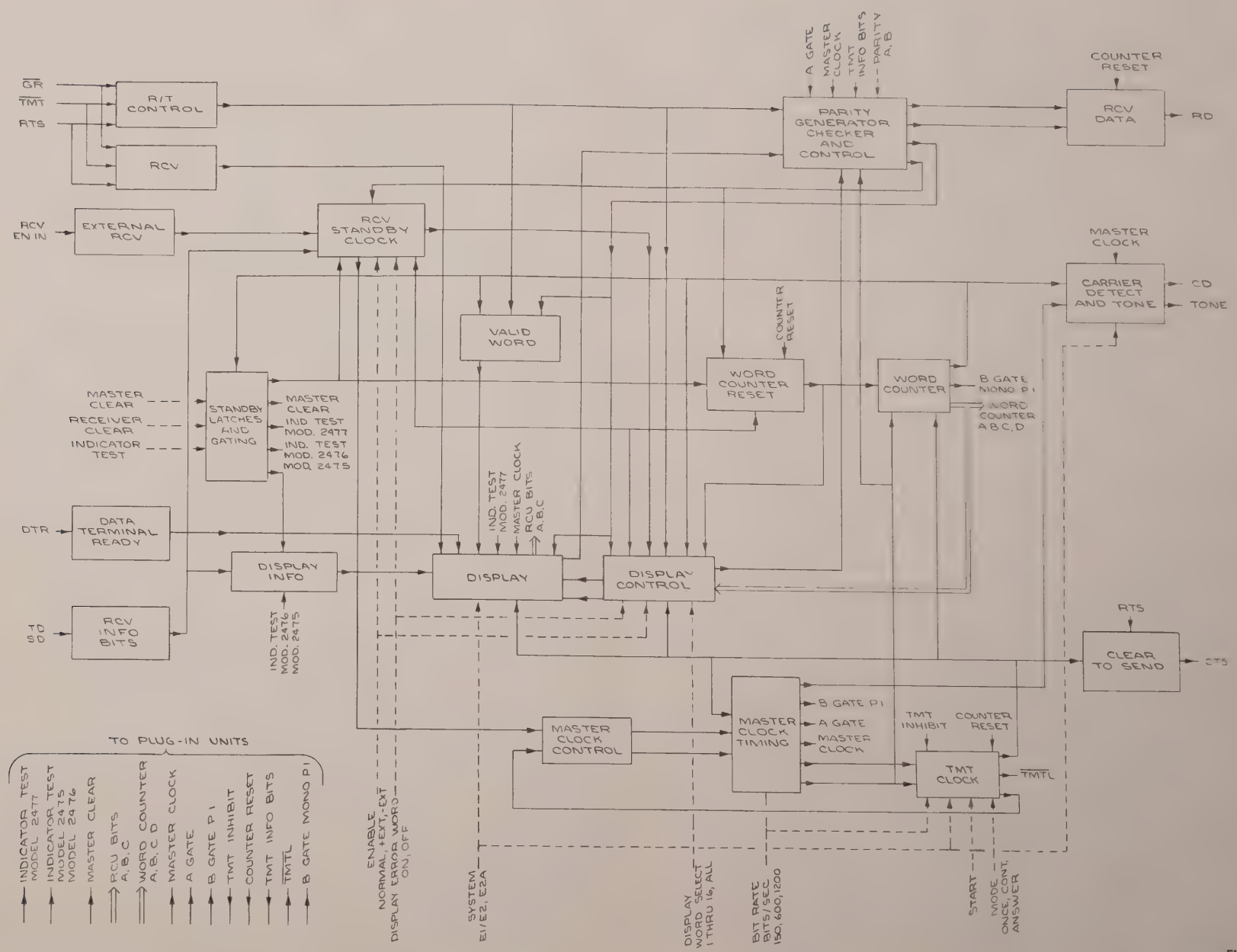


FIGURE 3-2
BLOCK DIAGRAM
MODEL 2474

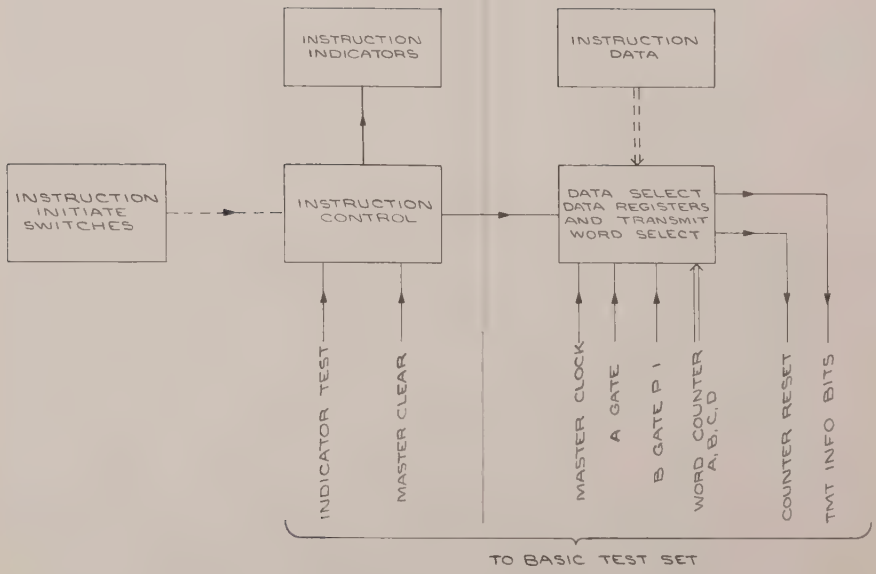


FIGURE 3-3
SIMPLIFIED BLOCK DIAGRAM
MODEL 2476

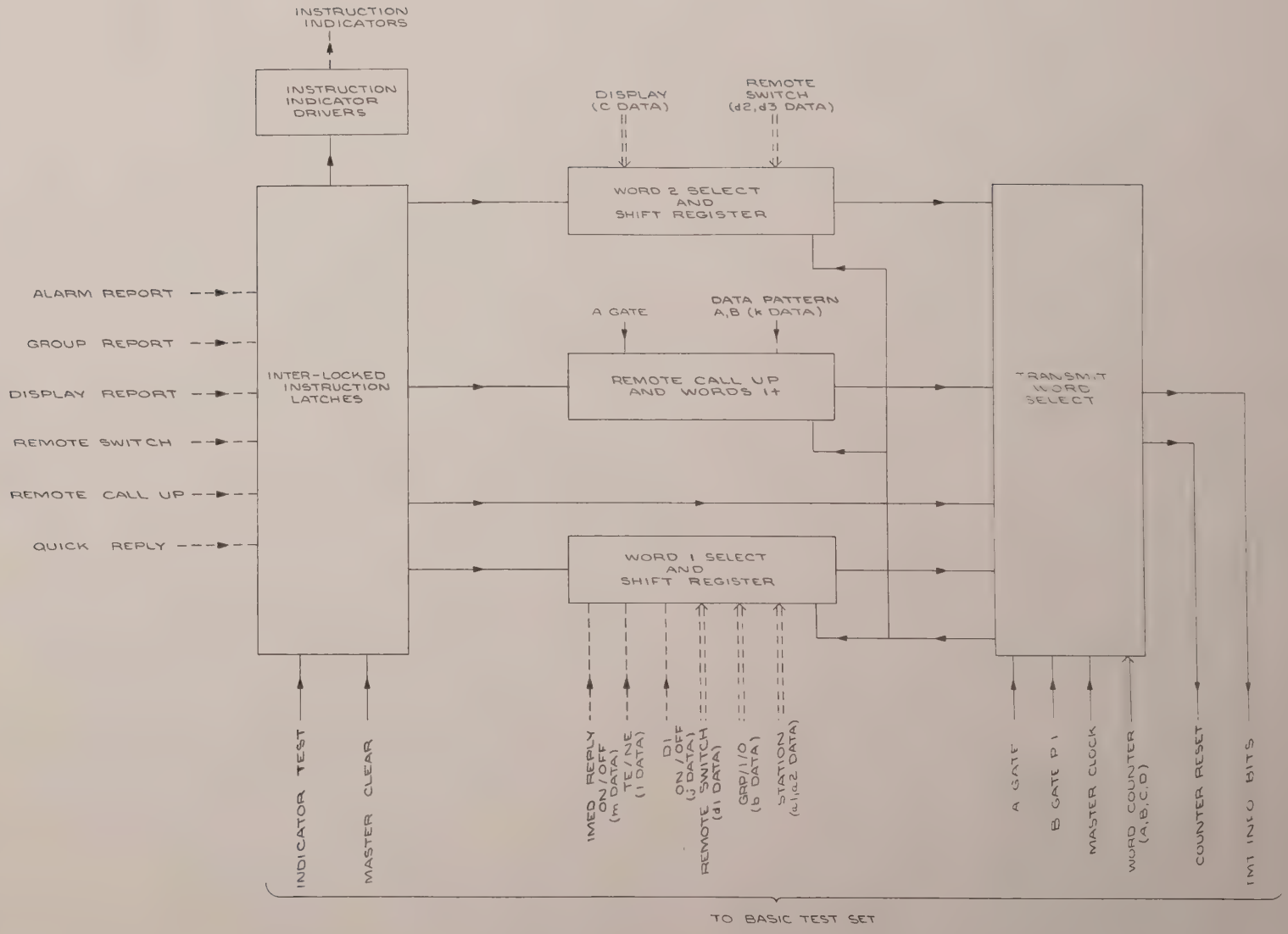


FIGURE 3-4
BLOCK DIAGRAM
MODEL 2476

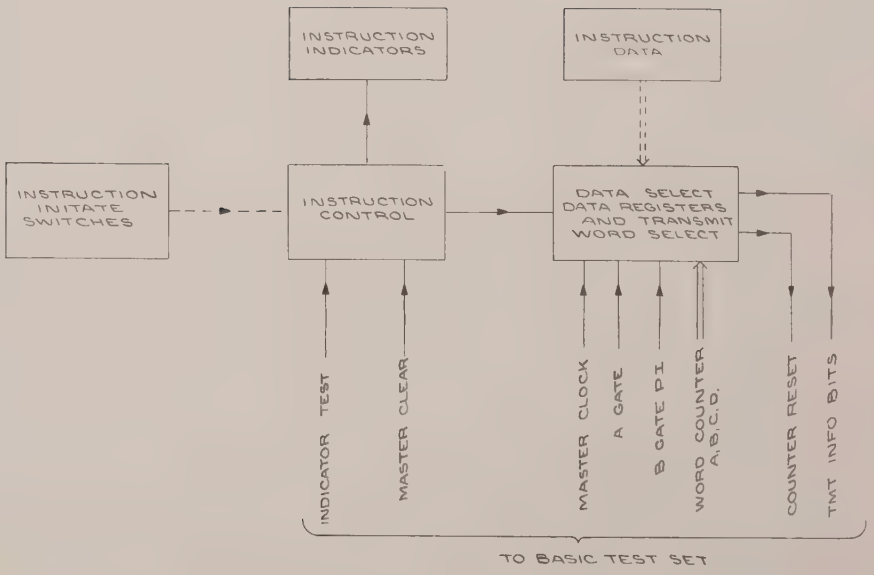


FIGURE 3-5
SIMPLIFIED BLOCK DIAGRAM
MODEL 2475

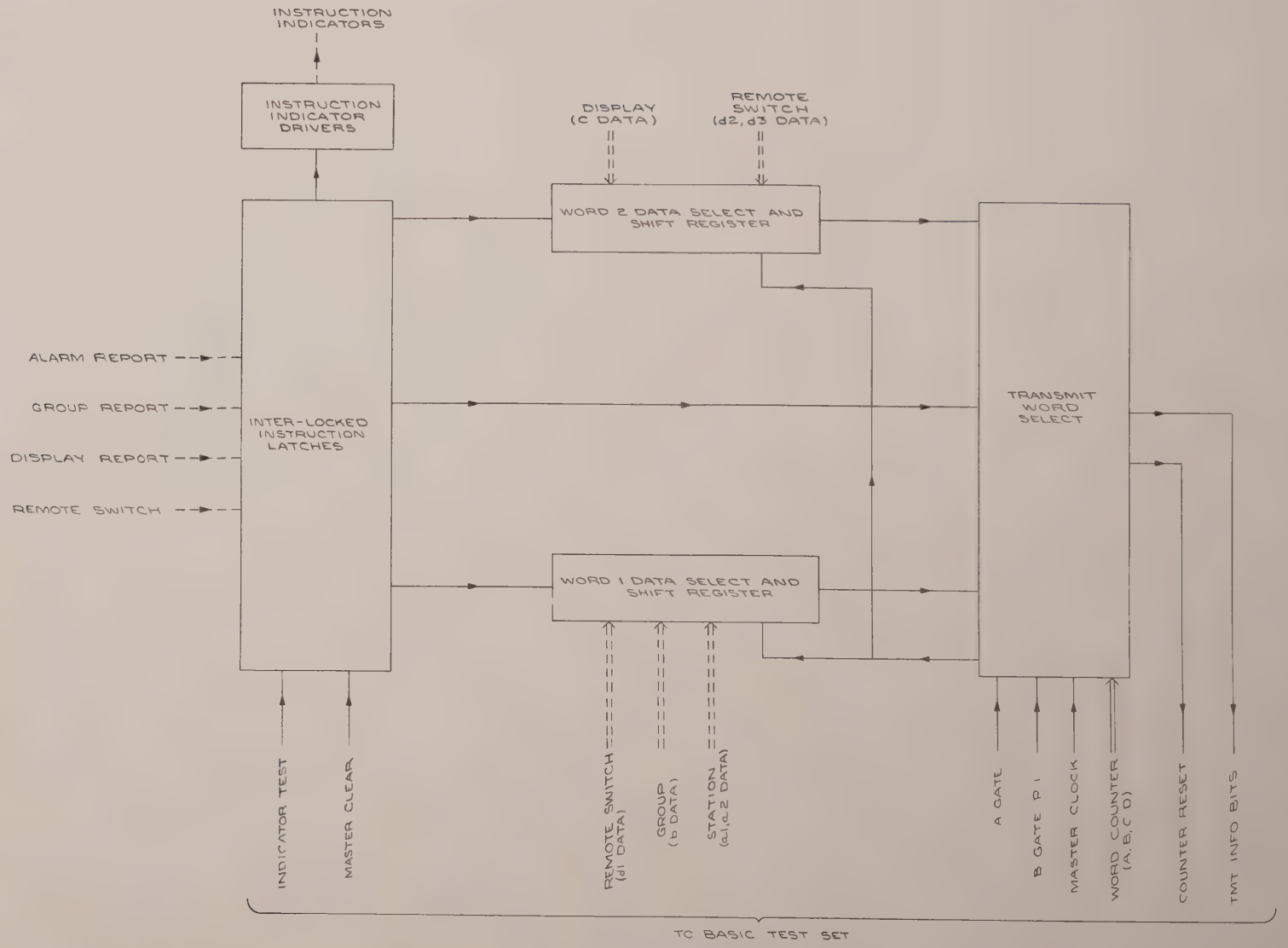


FIGURE 3-6
BLOCK DIAGRAM
MODEL 2475

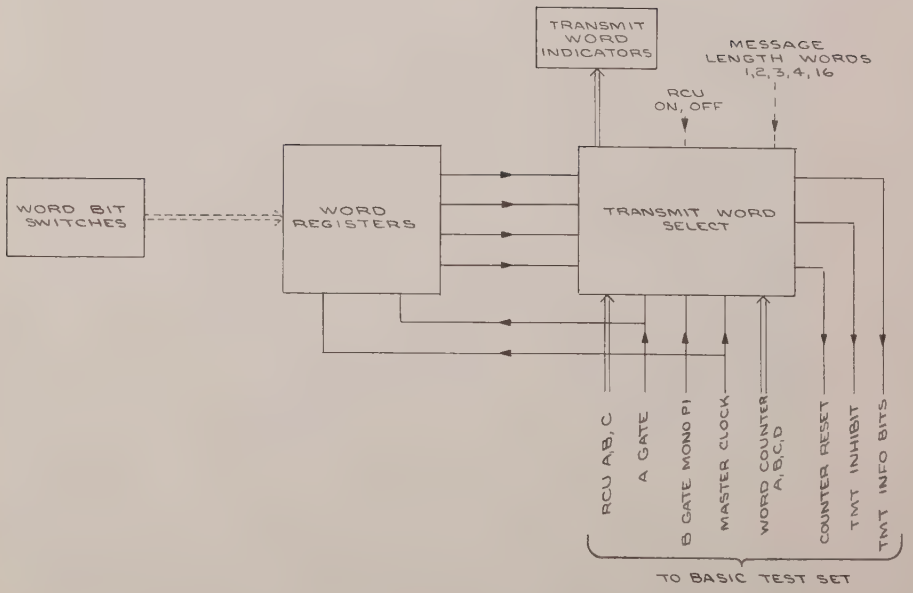


FIGURE 3-7
SIMPLIFIED BLOCK DIAGRAM
MODEL 2477

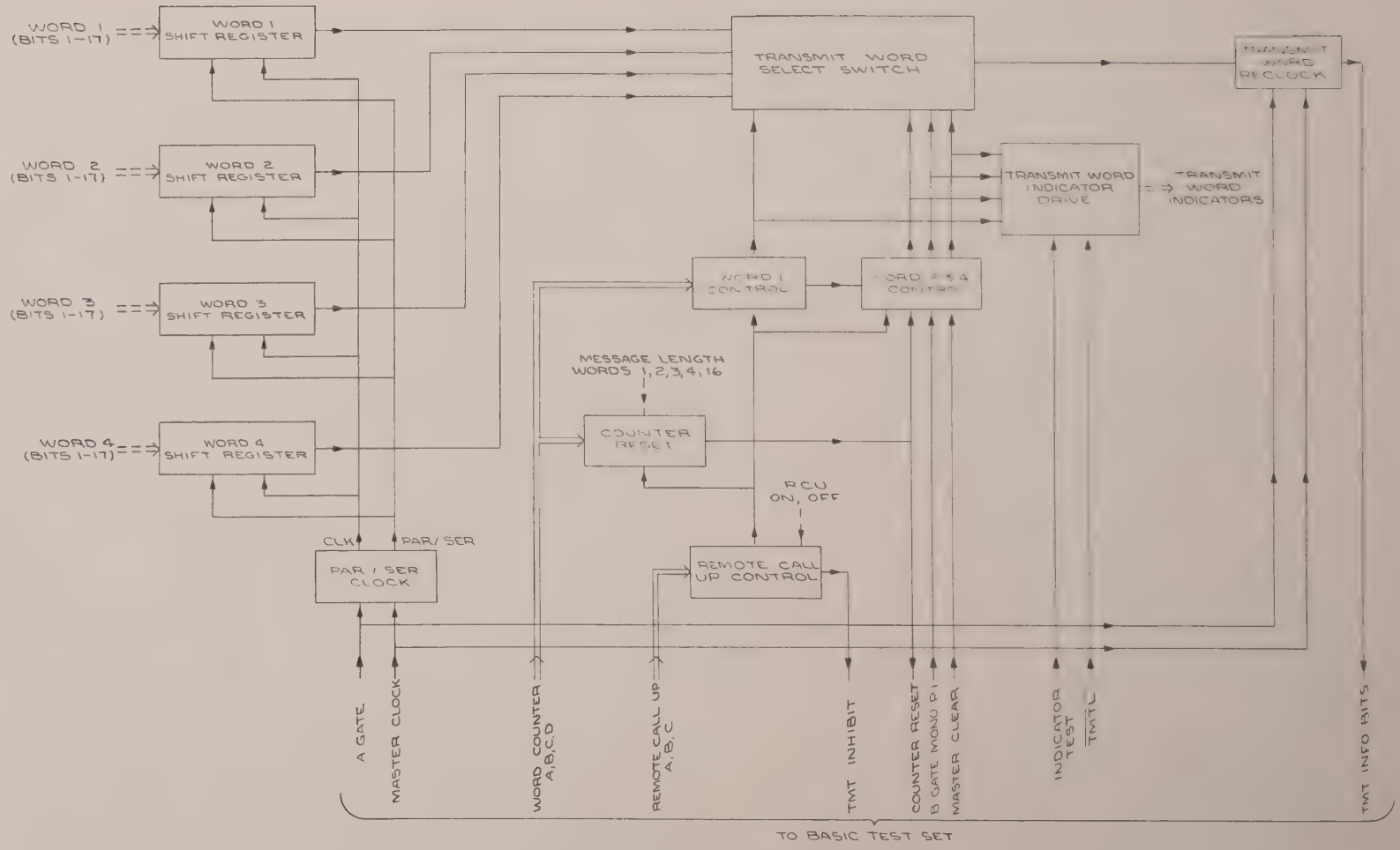


FIGURE 3-8
BLOCK DIAGRAM
MODEL 2477

Maintenance

4-1. AC POWER CAUTIONS

4-1a. When performing any preventive maintenance or repair it is advisable that the source of electric power be removed from the equipment to prevent a possible accidental shock.

4-1b. If the source of a problem has yet to be determined and trouble shooting is required with the equipment out of its cabinet, observe general safety precautions. The main precautions to be taken are:

1) Insure "proper grounding" of equipment.

2) Keep extremeties away from sources of dangerous potentials such as the AC power line.

4-2. MAINTENANCE INSTRUCTIONS

4-2a. Very little maintenance is required in the E-TELEMETRY STATION TEST SET equipment in that there are no coils, pots or other variable adjustments which must be periodically re-adjusted for peak performance.

4-2b. It is, however, recommended that all switches and controls which are not hermetically sealed be periodically sprayed with a general purpose lubricant contact spray (DO NOT USE SILICONE). Also the contact fingers of each plug-in printed circuit (P.C.) board should be coated with a light film of contact lubricant.

4-2c. After lubricating switches, turn them several times in each direction to "wipe" the contacts clean. If P.C. board fingers are sprayed insert and remove the board from its connector several times to both "wipe" the fingers and connector contacts.

4-2d. Inspect all hardware to insure that no nuts, lock washers, flat washers or bolts have loosened and have become sources for potential shorts.

Minor Repair Procedures

5-1. PURPOSE OF THIS SECTION

5-1a. The purpose of this section is to acquaint those involved in making printed circuit board repairs in this equipment with the proper technques to be used when soldering or unsoldering discrete components.

5-1b. Since most of the circuits utilize COS/MOS I.C.'s some helpful hints are included for removal and handling of these I.C. packages. Read this section in its entirety before attempting repair procedures.

5-2. DISCRETE COMPONENT REPLACEMENT OF P.C. BOARDS

5-2a. **General Steps To Be Followed:**

1) Disconnect all power to the equipment.

2) Remove all required covers on the module requiring repair.

3) Locate the defective component p.c. board.

4) Remove the p.c. board from its connector.

5) Since most p.c. boards contain COS/MOS I.C.'s, it is good general practice to short all fingers of the p.c. board together and to ground them while making repairs on the board.

6) Most discrete components mounted on p.c. boards have their leads bent flush with the foil on the opposite side of the board therefore it is **not** advisable to simply heat a lead and try to "pry the component out." Foil damage is most likely to occur since more than adequate heat would be required. Also mechanical damage could result to adjacent components via the "pry tool."

7) Use a standard **grounded** iron with an appropriate tip for p.c. board repairs. The iron's wattage should be about 25 watts.

8) Temporary heat sinking on leads of semi-conductor components whose junctions may be destroyed by excessive heat while soldering should be employed.

5-2b. Specific Steps To Be Followed

1) Apply enough heat to melt the solder around the lead to be removed and "suck" up the solder using a good commercially available solder evacuator.

2) Take care to avoid solder splashes as a bridge could cause further damage to components when operation is resumed.

3) Once the solder is removed, use a fine blade screw driver or similar tool to "break" the lead gently away from the foil.

4) Straighten the lead using a pair of needle nosed pliers.

5) In similar fashion perform the above precedures for the remaining leads of the component to be removed and then "remove" the component.

6) Observe polarities and lead positioning for the particular replacement component, if required, when reinserting them into the p.c. board.

7) If any spacers or insulators were used with the original component, remove them from the original and incorporate them with the new component.

8) Install the new component in a similar fashion as the one which was removed and solder into place.

9) Clean all flux and residue in the repaired area and surrounding areas using Tricholroethylene Reagent T-615 or equivalent.

5-3. COS/MOS I.C. REPLACEMENT AND HANDLING

5-3a. Follow all steps in paragraph 5-2a which are applicable. All I.C.'s however, **do not** have their leads bent over when they are inserted into the board. This practice should always be followed as well as the following.

1) When removing TTL as well as COS/MOS I.C.'s, remove the solder around each lead and gently nudge each lead until it is free from any foil contact.

2) Remove the I.C. from the board and replace **only** with the same type.

5-3b. The following information is presented to aquaint those unfamiliar with the handling of COS/MOS I.C.'s.

1) The input protection networks incorporated in most COS/MOS devices are effective in a wide variety of device handling situations. To be totally safe, however, it is desirable to restate the general conditions for eliminating all possibilities of device damage. Since COS/MOS devices have extremely high input resistance, they are susceptible to damage when exposed to extremely high static electrical charges. To avoid possible damage to the devices during handling, testing, or actual operation the following procedures should be followed:

a) The leads of devices should be in contact with a conductive material, except when being tested or in actual operation, to avoid build-up of static charge.

b) Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.

c) Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.

d) Signals should not be applied to the inputs while the device power supply is off.

e) All unused input leads must be connected to either V_{SS} (ground) or V_{DD} (supply voltage), whichever is appropriate for the logic circuit involved.

Table 5-1 indicates general handling procedures recommended to prevent damage from static electrical charges.

2) Handling Of Subassembly Boards —

After COS/MOS I.C. 's have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice during processing operations to put conductive clips or conductive tape on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on the board.

All normal flux removing and degreasing solvents can be used without adversely affecting the reliability of COS/MOS plastic devices.

3) Soldering Time and Temperature —

All device leads can withstand exposure to temperature as high as 265°C for 10 sec, MAX. and as close as 1/16 ± 1/32 inch from the body of the device.

4) Storing of Printed-Circuit Boards —

Excessive humidity (greater then 60%) should be avoided during circuit-board check-out to prevent the false impression of excessive device internal leakage. High relative humidity may cause leakage paths between closely spaced elements of the circuit boards, such as the terminals and insulated metallized connection strips. Normally this added leakage is not significant in non-COS/MOS devices. However, when the nanoampere-leakage advantages of COS/MOS devices are desired, leakage currents on circuit boards or non-hermetic modules which are affected by high humidity become of major concern and must be controlled by coating, cleaning or better environmental controls.

TABLE 5-1 GENERAL HANDLING CONSIDERATIONS

	Should be conductive	Should be grounded to common point
Metal Parts of Fixtures and Tools		X
Handling Trays	X	X
Soldering Irons		X
Table Tops	X	X
Transport Carts		(Static Discharge Straps)
Manufacturing Operating Personnel		*(Utilize grounded metal wrist straps)
General Handling of Devices		*(Utilize grounded metal wrist straps)

Total protection results when personnel and materials are all at the same or ground potential.

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exceptions.

*1-megohm series resistor.

Troubleshooting

6-1. SCOPE OF THIS SECTION

This section describes the troubleshooting techniques for the E-Telemetry Station Test Set. The information consists of a logical troubleshooting procedure in tabular form and applicable waveforms Figures 6-1 through 6-18. Refer to TABLE 6-1 Troubleshooting Chart, Block Diagrams in Section 3, Schematic Drawings in Section 7 and the following illustrations.

Figure 2-1 CONTROL, INDICATORS AND CONNECTOR LOCATIONS, MODEL 2474

Figure 2-2 CONTROL, INDICATORS AND CONNECTOR LOCATIONS, MODEL 2476

Figure 2-3 CONTROL, INDICATORS AND CONNECTOR LOCATIONS, MODEL 2475

Figure 2-4 CONTROL, INDICATORS AND CONNECTOR LOCATIONS, MODEL 2477

6-1a. LOGICAL TROUBLESHOOTING

Troubleshooting procedures presented in this section are based on the following six logical steps:

6-1b. SYMPTON RECOGNITION

This is the first step in the troubleshooting procedures and is based on a complete knowledge and understanding of the equipment operating characteristics. Because visual indicators are an integral part of the circuitry, 'the trouble is frequently apparent from the presentation. All equipment troubles are not the direct result of a component failure and are not always easy to recognize, since all conditions of less than peak performance are not always apparent. Degradation in equipment performance is usually detected during preventive maintenance procedures. It is important that the "not so apparent" troubles as well as the apparent troubles be recognized.

6-1c. SYMPTON ELABORATION

After an equipment trouble has been "recognized" all available built-in troubleshooting aids should be utilized to elaborate on the original trouble sympton. Use of front panel controls and built-in data indicator presentations may provide better identification of the original trouble symptom. For example, a clocking failure symptom may be elaborated upon by changing the BIT RATE to see if it is dependent upon switch settings. Frequently narrowing down the probable trouble area results with this technique. Also, checking or otherwise exercising the front panel controls may reveal that incorrect settings exist which have been overlooked.

6-1d. LISTING PROBABLE FAULTY FUNCTION

The next step in logical troubleshooting is to formulate a number of "logical choices" as to the cause and likely location (functional section) of the trouble. The "logical choices" are mental decisions which are based on a knowledge of the equipment operation, a full identification of the trouble symptom, and information contained in this manual. The overall functional description and its associated block diagram should be referred to when selecting possible faulty functional sections. For example, the logical choice based on the symptoms in paragraph c would be the Master Clock & Timing circuits.

6-1e. LOCALIZING THE FAULTY FUNCTION

For the greatest efficiency in localizing trouble, the functional sections which have been selected by the logical choice method should be tested in an order that will require the least time. This requires a mental selection to determine which section to test first. The selection should be based on the validity of the logical choice and the difficulties in making the necessary tests. If the tests do not prove that functional section to be at fault, the next selection should be tested, and so on until the faulty functional section is located. As

aids in this process, this section contains waveforms for each functional section. Also, test data (such as information on control settings) are included to augment the description of each functional section.

6-1f. LOCALIZING TROUBLE TO THE CIRCUIT

Once the faulty functional section has been isolated, the task of localizing trouble to a circuit level becomes a matter of signal tracing the suspected functional section. Toward this end, standard signal tracing methods should be employed, e. g., voltages and/or waveforms should be traced throughout the functional section, starting at the input and working towards the output of that section. Once the defective circuit is localized, the next step is replacement of a circuit board or component on a board. A normally functioning circuit is proof of proper fault isolation. The block diagrams, schematic diagrams and their associated discussions are provided for troubleshooting at the circuit level. These diagrams and discussions are found in Sections 6 and 7.

6-1g. FAILURE ANALYSIS

Before performing the actual repair or corrective action, review the process which led to the faulty component to determine why the fault caused the symptoms it did. In some cases a review of the process may prove that the faulty component is a result of a failure instead of the failure itself. In this instance, further troubleshooting is required. The review and proper failure records will also prove a valuable case history for future equipment failures.

6-2 SUGGESTED TEST EQUIPMENT

-Dual channel oscilloscope. Tektronix Type 453 or equivalent -Volt-ohmmeter, Triplett Model 630 or equivalent-Frequency counter, Monsanto Model 100A or equivalent. It should be noted that a second working Model 2474, Basic Test Set, and Model 2477, General Purpose Plug-In, together can serve as a most valuable piece of test equipment, since the Station Test Set can be operated independent of possibly faulty station equipment.

6-3 TROUBLESHOOTING CHART

Table 6-1 Troubleshooting Chart, Station Test Set, lists symptom, probable cause and remedy to aid in the troubleshooting process.

TABLE 6-1 TROUBLESHOOTING CHART, STATION TEST SET

SYMPTOM	PROBABLE CAUSE	REMEDY
1. Power Indicator does not light when Power switch is ON.	a. Unit not plugged in	a. Check a.c. line connection
	b. Defective fuse	b. Change fuse **CAUTION** If fuse burns out again do not replace fuse until problem is located. Unplug unit check for short circuits.
	c. Defective lamp	c. Replace lamp if defective.
	d. Defective VR3 Board 9009	d. Replace VR3 **CAUTION** Before replacing VR3 unplug boards 9005 through 9008. If POWER indicator remains off replace VR3.
	e. Defective +9.5 v power supply	e. Perform voltage and resistance checks to locate faulty power supply components on board 9009.
2. All indicators will not clear when MASTER CLEAR is depressed.	a. Defective switch	a. Replace switch
	b. Master Clock malfunction	b. Check board 9003 IC5 and associated circuitry. Check board 9002, refer to Waveforms Master Clock, Figure 6-2.
Receive indicators will not clear when RECEIVER CLEAR is depressed	c. Display Info incorrect.	c. Check board 9001, refer to Waveforms Receive Logic, Figure 6-1.
All indicators will not light when INDICATOR TEST is depressed.	d. Display malfunction	d. Check board 9010
	e. Station Test Set is receiving.	e. Operation normal

TABLE 6-1 TROUBLESHOOTING CHART, STATION TEST SET (Continued)

SYMPTOM	PROBABLE CAUSE	REMEDY
3. RCV Lamp indicates receive no data displayed	a. Receive Logic malfunction	a. Check board 9001, refer to waveforms, Receive logic, Figure 6-1.
	b. Receive Info Bits malfunction	b. Check board 9008. Refer to Waveforms Interface II Figure 6-8.
	c. EXT EN IN malfunction	c. Check board 9008. Refer to Waveforms Interface II Figure 6-8.
	d. DISPLAY ERROR WORD switch in ON and ERROR WORD indicator is also on.	d. Turn DISPLAY ERROR WORD to OFF, Depress MASTER CLEAR or RECEIVER CLEAR.
	e. Display control malfunction	e. Check boards 9005 and 9006, refer to Waveforms $\overline{\text{RCV WORD}}$/ Buffer Figure 6-5 and Waveforms word Counter & Display control Figure 6-6.
	f. Position of DISPLAY WORD SELECT Switch greater than message length.	f. Turn DISPLAY WORD SELECT to ALL.
4. ERROR WORD constantly illuminated	a. PARITY switch in wrong position.	a. Select proper parity.
	b. Parity Generator/Checker Control malfunction.	b. Check board 9004, refer to Waveforms, Parity Generator/ Checker, Control, Figure 6-4.
	c. Display malfunction.	c. Check board 9010.
5. Receive indicators exhibit erratic behavior.	a. Bit Rate and data rate incompatible.	a. Check BIT RATE Switch.
6. Transmit does not occur when START is depressed	a. Defective switch	a. Replace switch
	b. Transmit Logic malfunction.	b. Check board 9003, refer to Waveforms, Transmit Logic, Figure 6-3.
7. TMT indicator goes on and remains on when START is depressed.	a. Counter Reset not being made, defective plug-in.	a. Refer to Circuit Descriptions and Schematic Diagrams for plug-in in use.
	b. Transmit Logic malfunction.	b. Check board 9003, refer to Waveforms, Transmit Logic, Figure 6-3.
8. Transmit Words in error.	a. Transmit word programming in error-defective plug-in.	a. Refer to Circuit Descriptions and Schematic Diagrams for plug-in in use.
	b. Parity generation in error.	b. Check board 9004, refer to Waveforms, Parity Generator/ Checker Control, Figure 6-4.
	c. Transmit word voltage levels incorrect.	c. Check board 9007, Interface I, refer to Waveforms Interface I, Figure 6-7.

6-4 SUGGESTED TEST FIXTURE

If, in the process of troubleshooting, the station equipment becomes suspect, then the station test set can be operated independent of the station equipment to further isolate the problem area. In order to implement independent test set operation it is recommended that a test fixture be constructed to simulate station to station test set control lines and to provide test points for viewing station test set to station signals. TABLE 6-2 Test Fixture Signals and Interface Connection set forth the control signals, signals to be observed and the test fixture to station test set interface connections.

Refer to Table 1-1 Performance Specifications in Section 1 for proper levels to be generated by the test Fixture for the following signals: $\overline{TMT}$, $\overline{GR}$, RTS, TD, SD, and DTR. Table 1-1 also provides the proper levels for the following signals: TONE, CD, CTS, RD E1/E2 and RD E2A. Circuit description and waveforms for board 9007 provide timing information useful in determining if the Station Test Set to Test Fixture signals are correct.

The Test Fixture may be used in the following manner to determine if the Station Test Set is functioning properly.

1. Set $\overline{TMT}$ to logic 0, observe that RCV indicator is illuminated.

2. Set $\overline{GR}$ to logic 0, observe that RCV indicator is illuminated.

3. Set RTS to logic 1, observe that RCV indicator is illuminated.

4. Set DTR to logic 1, observe that DTR indicator is illuminated.

5. Transitions RTS from logic 0 to logic 1 observe CTS.

6. Set BTS controls as follows: SYSTEM Switch to E2A, PARITY Switch to A, DISPLAY WORD SELECT Switch to ALL, and ENABLE Switch to NORMAL. Set RTS to logic 1 and transition TD, SD from logic 1 to logic 0. Observe that the bit indicators are at logic 0 and a flicker of VALID WORD lamp occurs.

7. Set PARITY to B, transition TD, SD from logic 1 to logic 0. Observe that the bit indicators are at logic 0 and the ERROR WORD lamp is illuminated.

8. Set BTS and Plug-In to transmit continuously a 2 word message. Observe TONE, CD, RD E1/E2 and RD E2A.

9. Set BTS transmit MODE Switch to ANSWER, transition RTS from logic 1 to logic 0 observe that the message programmed in the Plug-In is transmitted once.

TABLE 6-2 TEST FIXTURE SIGNALS AND INTERFACE CONNECTION

TEST FIXTURE TO STATION TEST SET	STATION TEST SET TO TEST FIXTURE	INTERFACE CONNECTIONS
$\overline{TMT}$		P2 Pin 4
$\overline{GR}$		5
RTS		11
TD, SD		6
DTR		8
GRD	GRD	7
	TONE	3
	CD	10
	CTS	12
	RD E1/E2	2
	RD E2A	13

6-5 TROUBLESHOOTING USING SECOND MODELS 2474 & 2477

As mentioned previously, in paragraph 6-2, if a second Model 2474 BTS and Model 2477 Plug-In are available they can be utilized as test equipment when connected as per Table 6-3 Test Set/Test Set Inter-Connections.

TABLE 6-3 TEST SET/TEST SET INTER-CONNECTIONS

BTS # 1	BTS # 2
J2 pin 13 RD E2A	J2 pin 6 TD, SD
pin 6 TD, SD	pin 13 RD E2A
pin 10 CD	pin 11 RTS
pin 11 RTS	pin 10 CD
pin 1 GRD	pin 1 GRD

When 2 test sets are inter-connected in the above fashion all capabilities of each unit can be exercised and monitored fully.

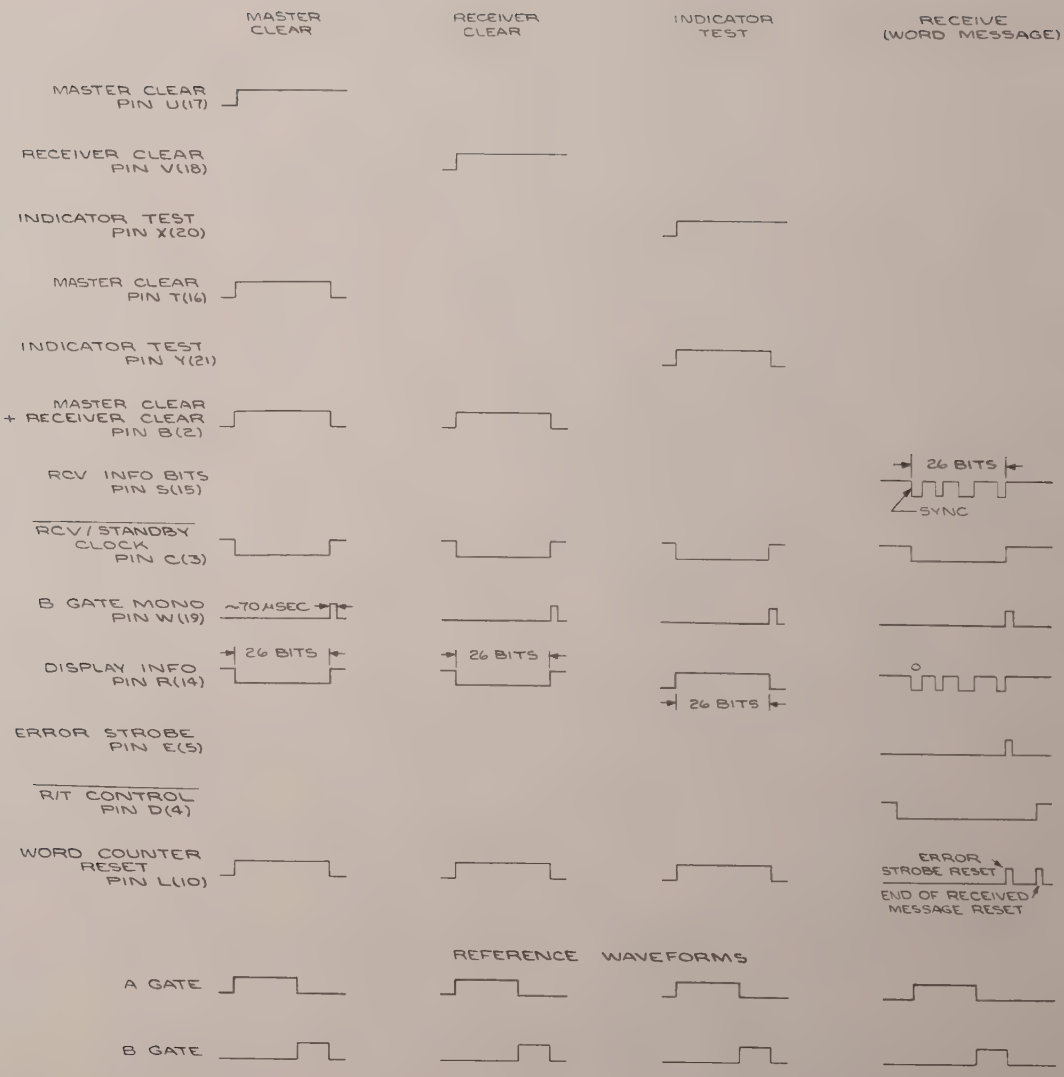
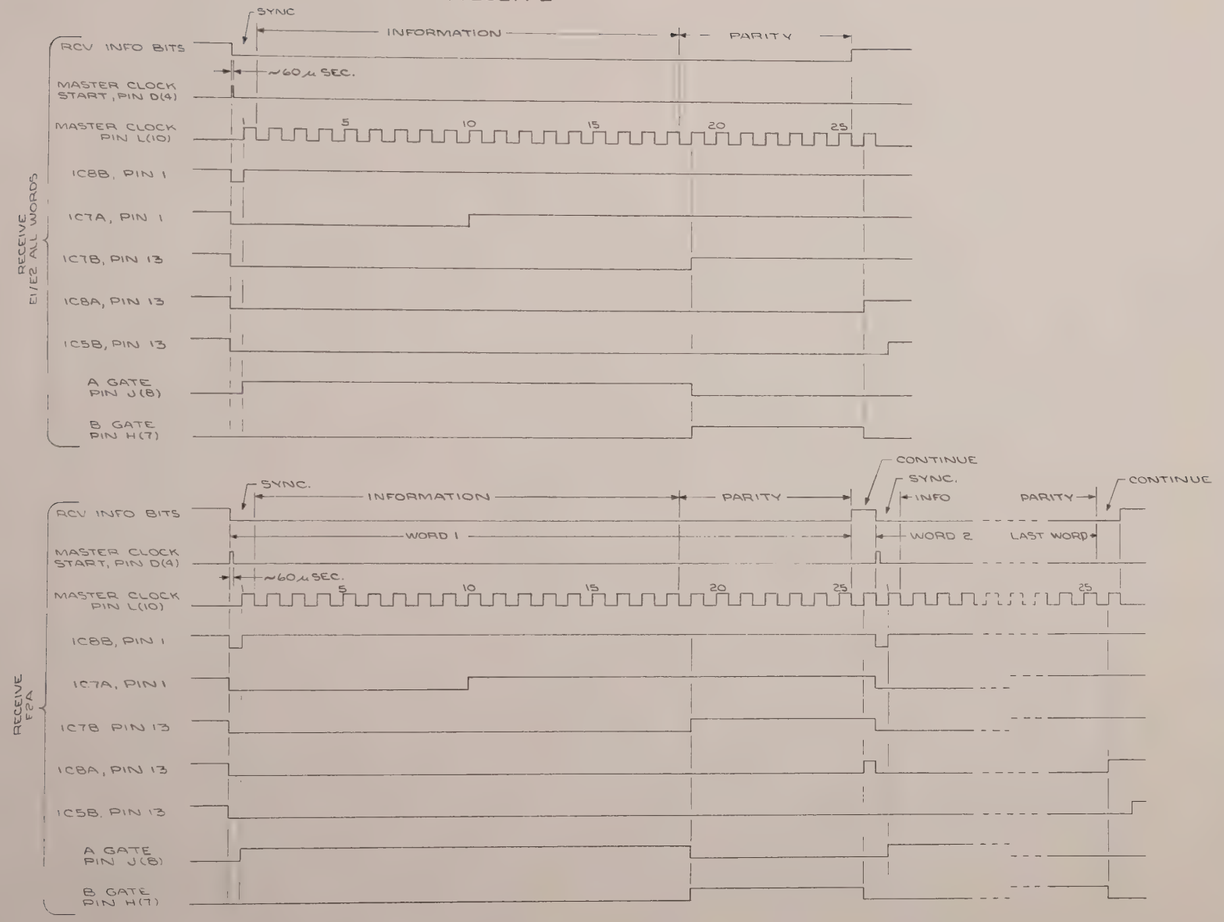


FIGURE 6-1
WAVEFORMS
BOARD 9001
RECEIVE LOGIC
MODEL 2474



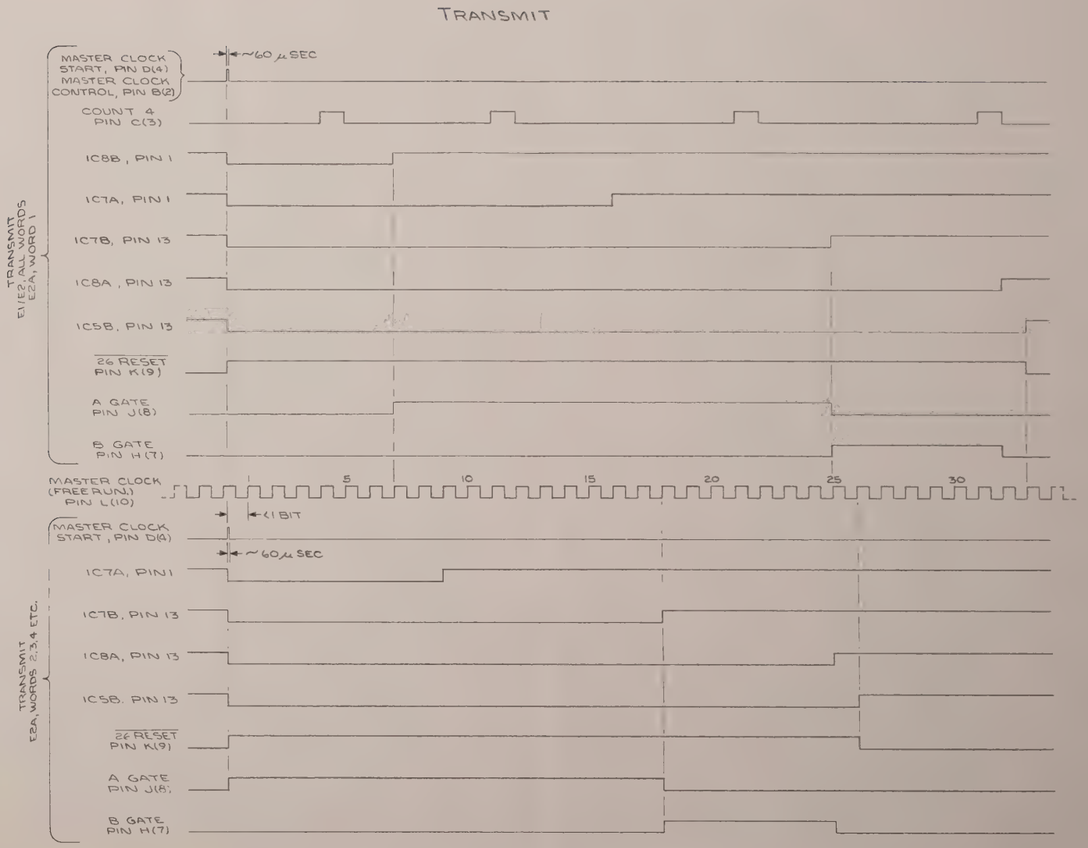


FIGURE 6-2
WAVEFORMS
BOARD 9002
MASTER CLOCK
MODEL 2474

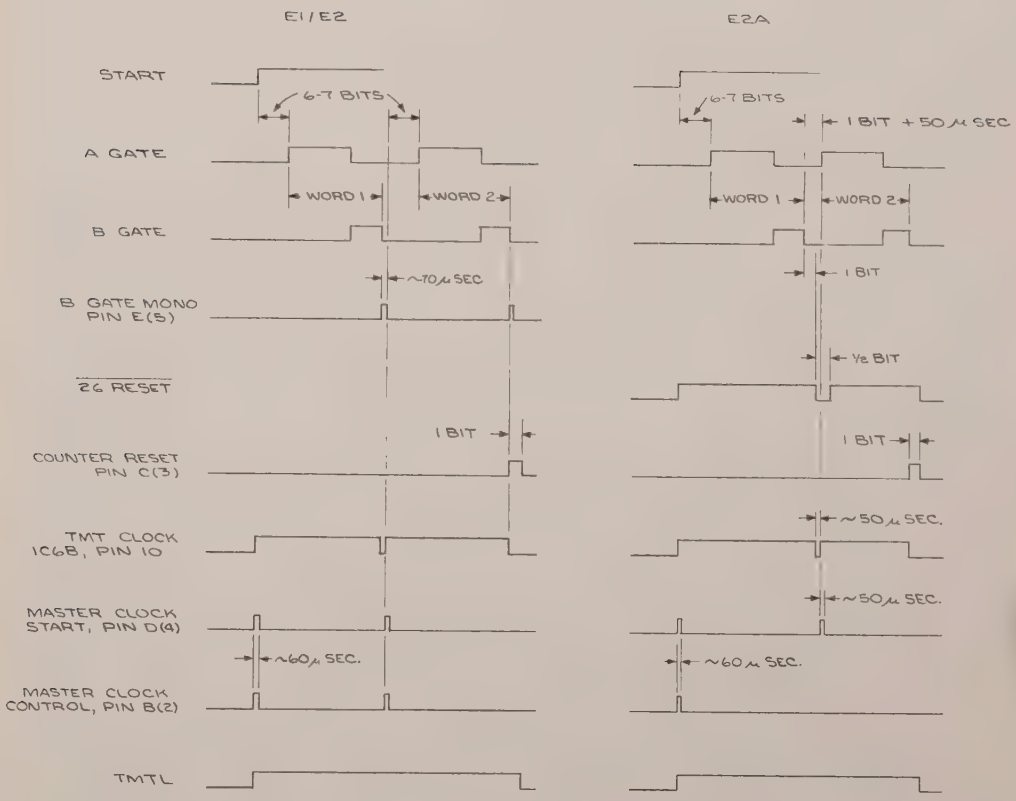


FIGURE 6-3
WAVEFORMS
BOARD 9003
TRANSMIT LOGIC
MODEL 2474

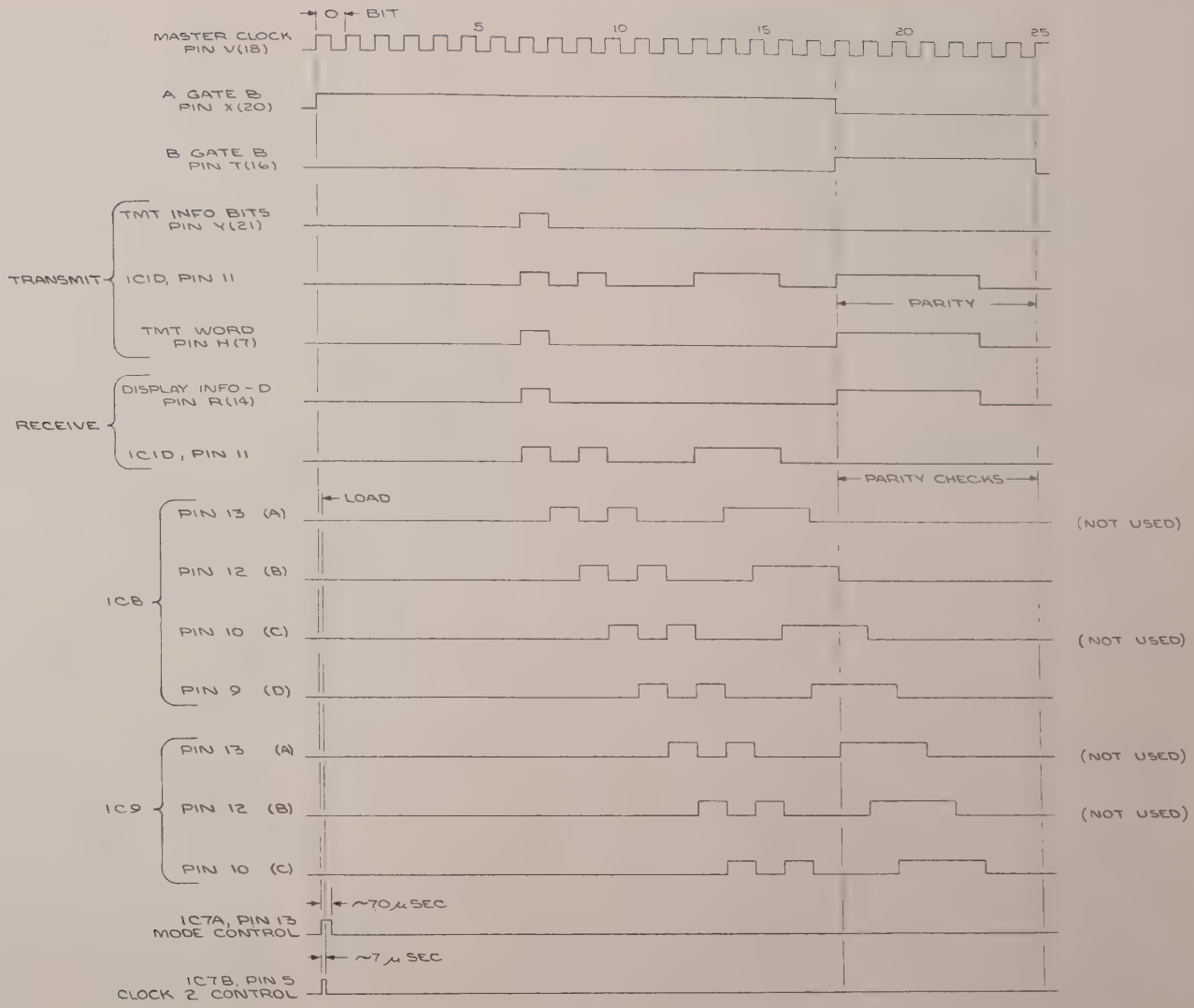


FIGURE 6-4
WAVEFORMS
BOARD 9004
PARITY GENERATOR/CHECKER, CONTROL
MODEL 2474

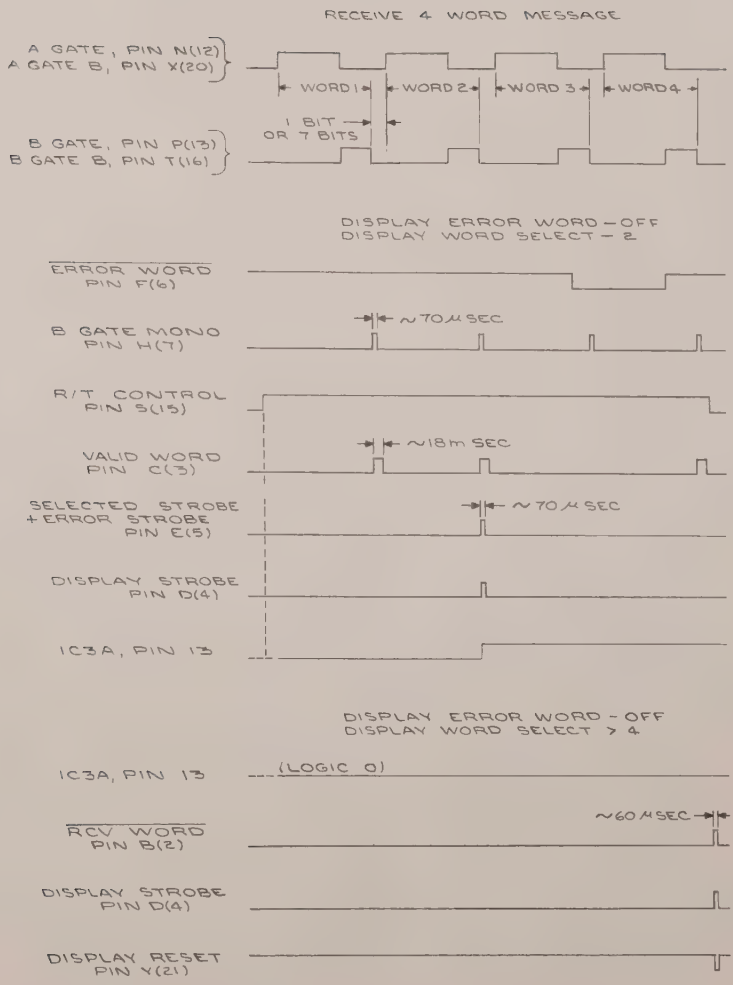


FIGURE 6-5
WAVEFORMS
BOARD 9005
RCV WORD/BUFFER
MODEL 2474

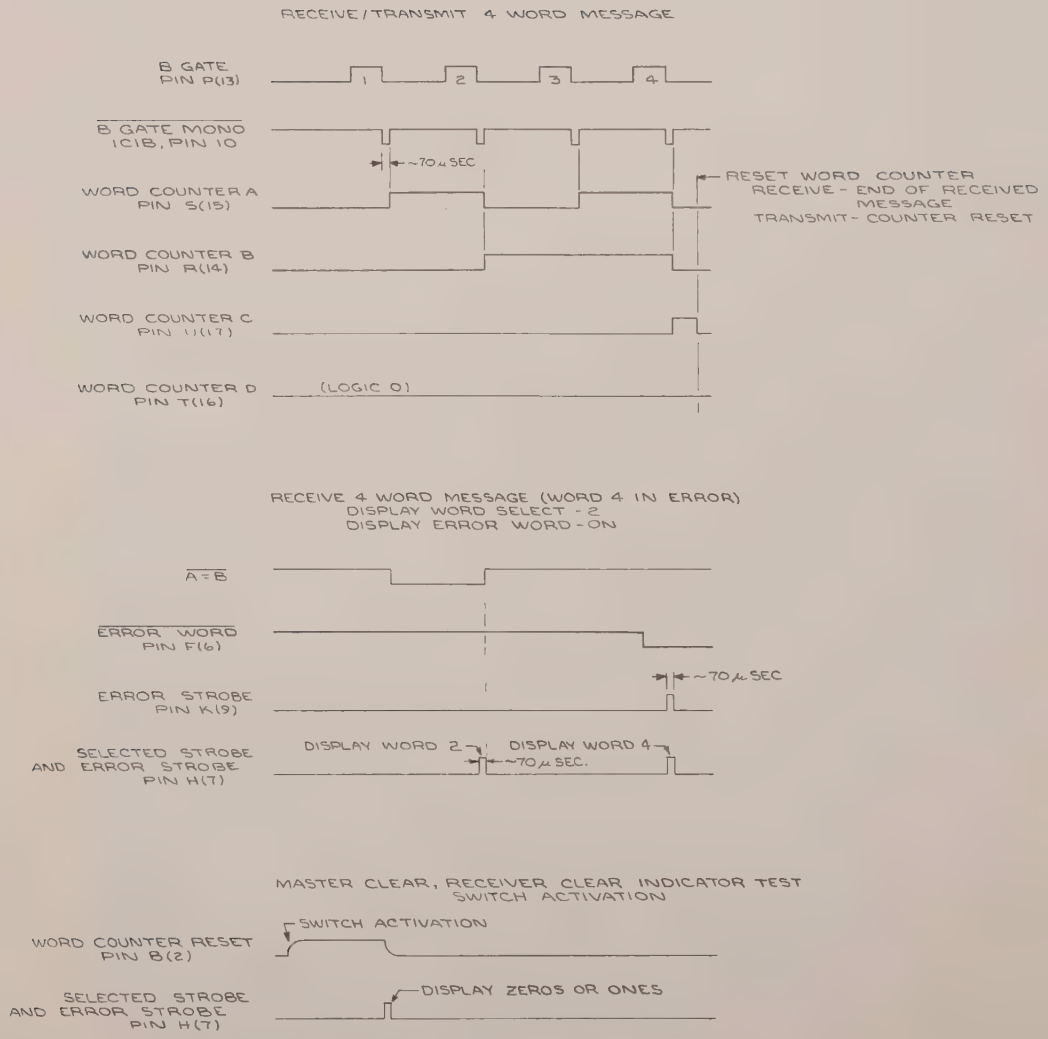


FIGURE 6-6
WAVEFORMS
BOARD 9006
WORD COUNTER AND DISPLAY CONTROL
MODEL 2474

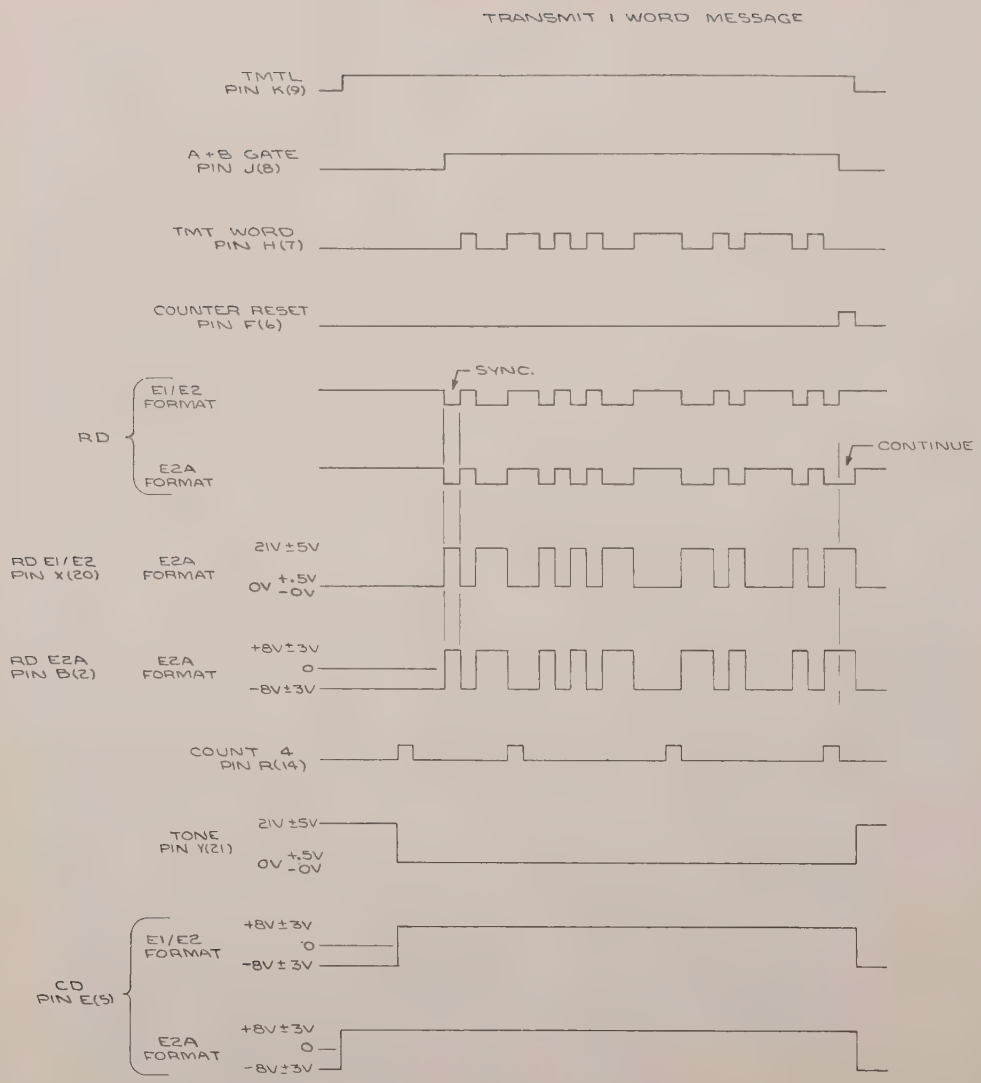


FIGURE 6-7
WAVEFORMS
BOARD 9007
INTERFACE I
MODEL 2474

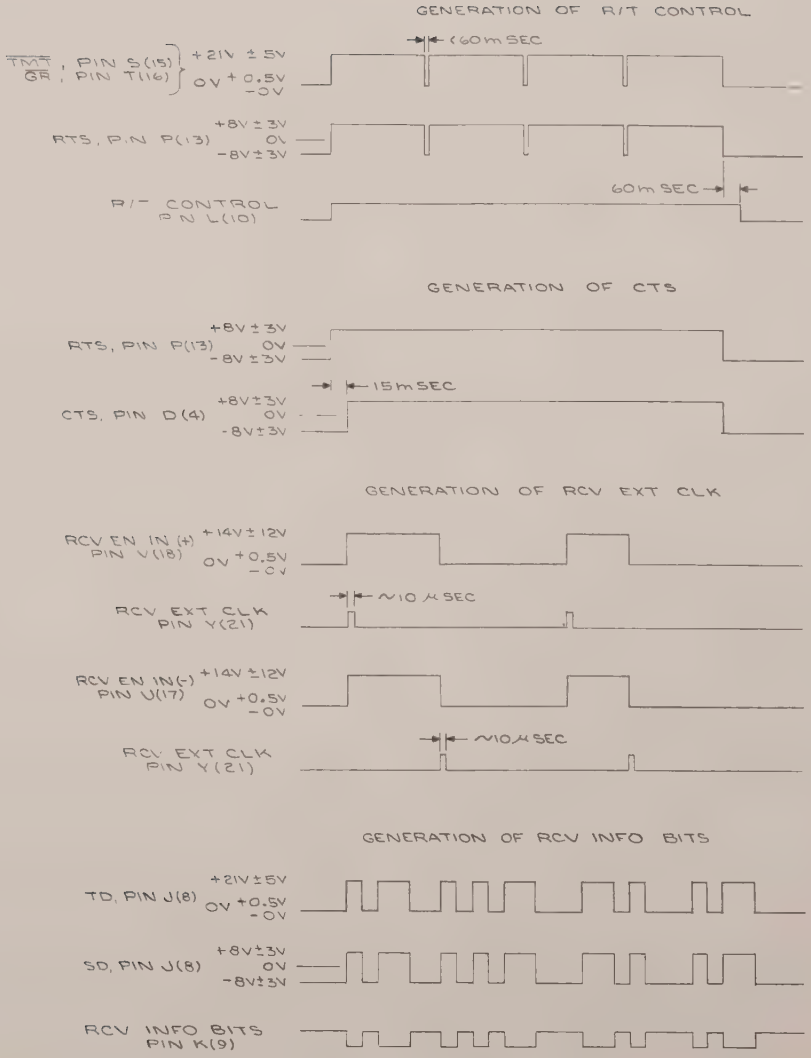


FIGURE 6-8
WAVEFORMS
BOARD 9008
INTERFACE II
MODEL 2474

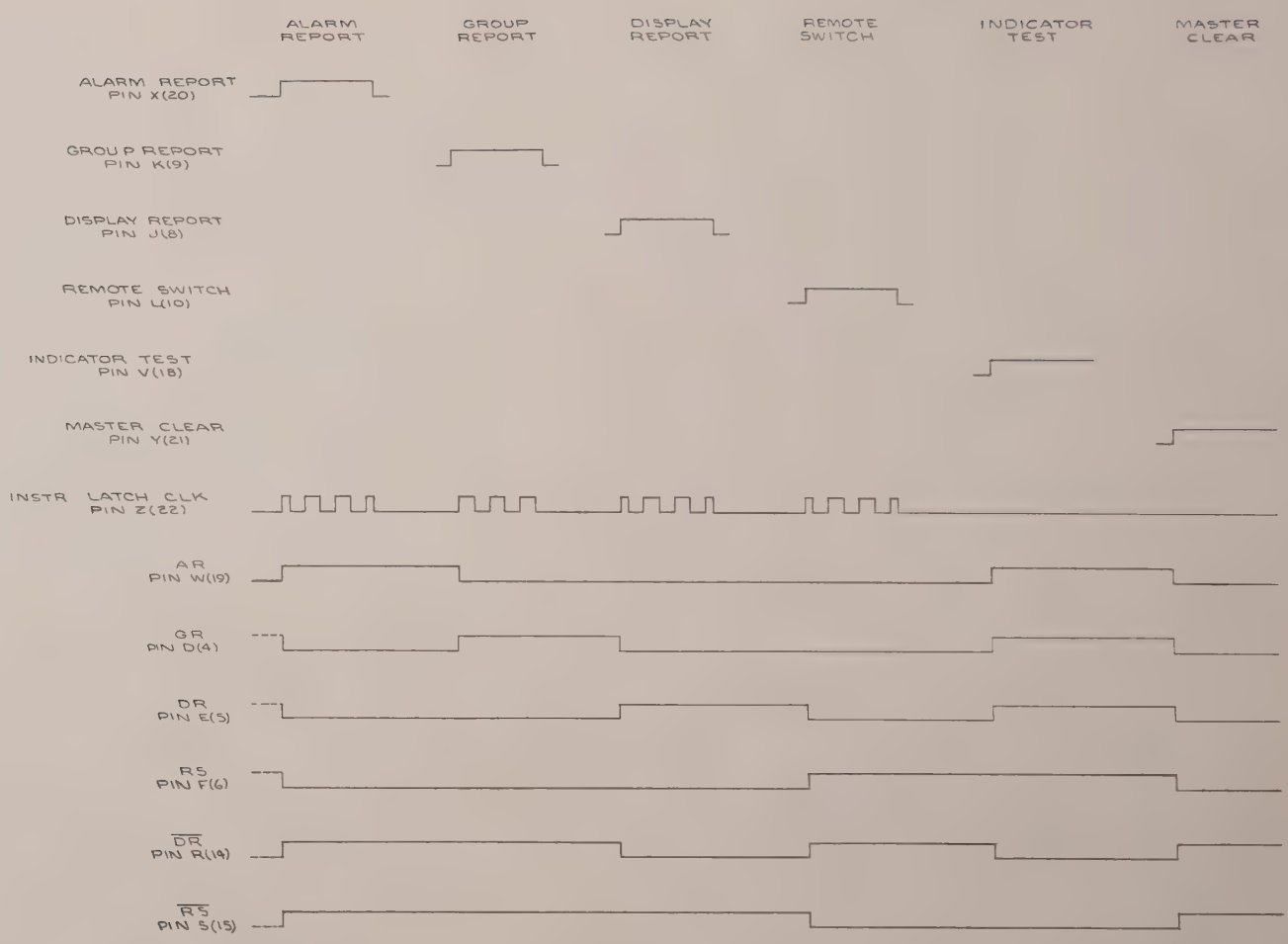


FIGURE 6-9
WAVEFORMS
BOARD 9051
INSTRUCTION CONTROL LOGIC I
MODEL 2476

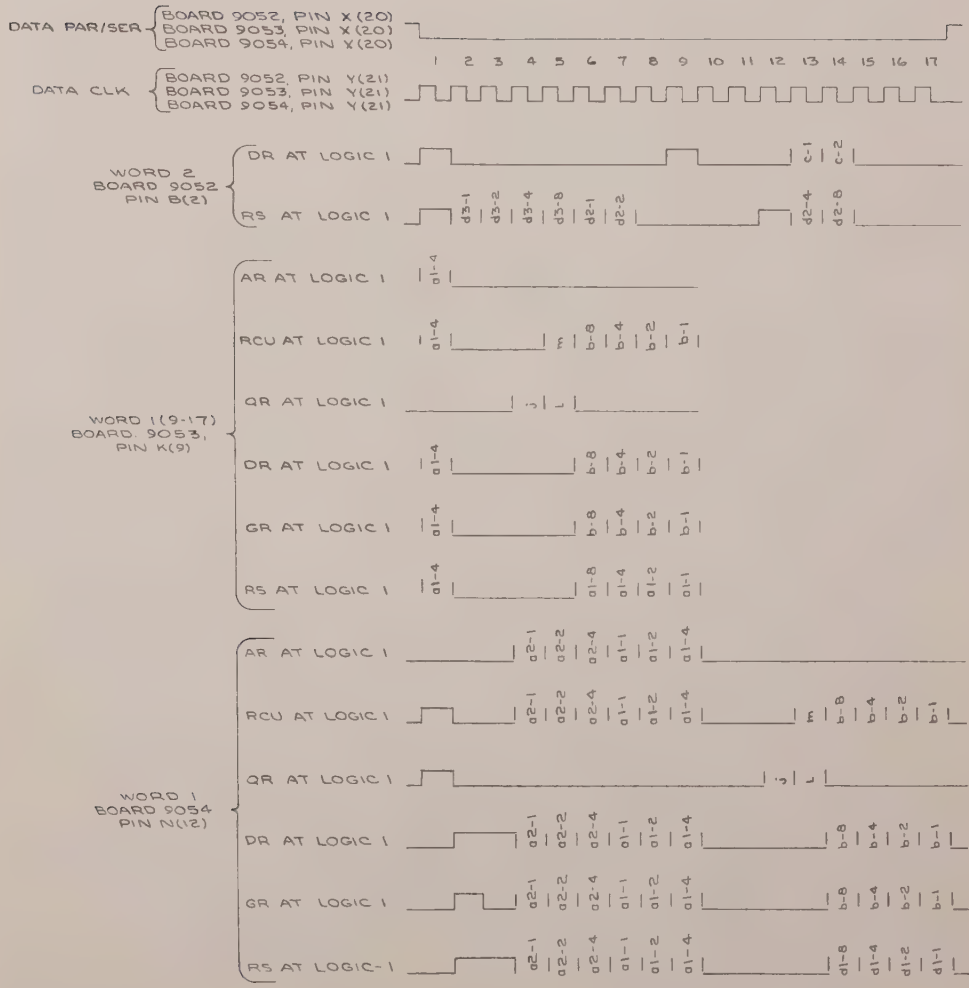


FIGURE 6-10
WAVEFORMS
BOARDS 9052, 9053, 9054
WORD REGISTERS
MODEL 2476

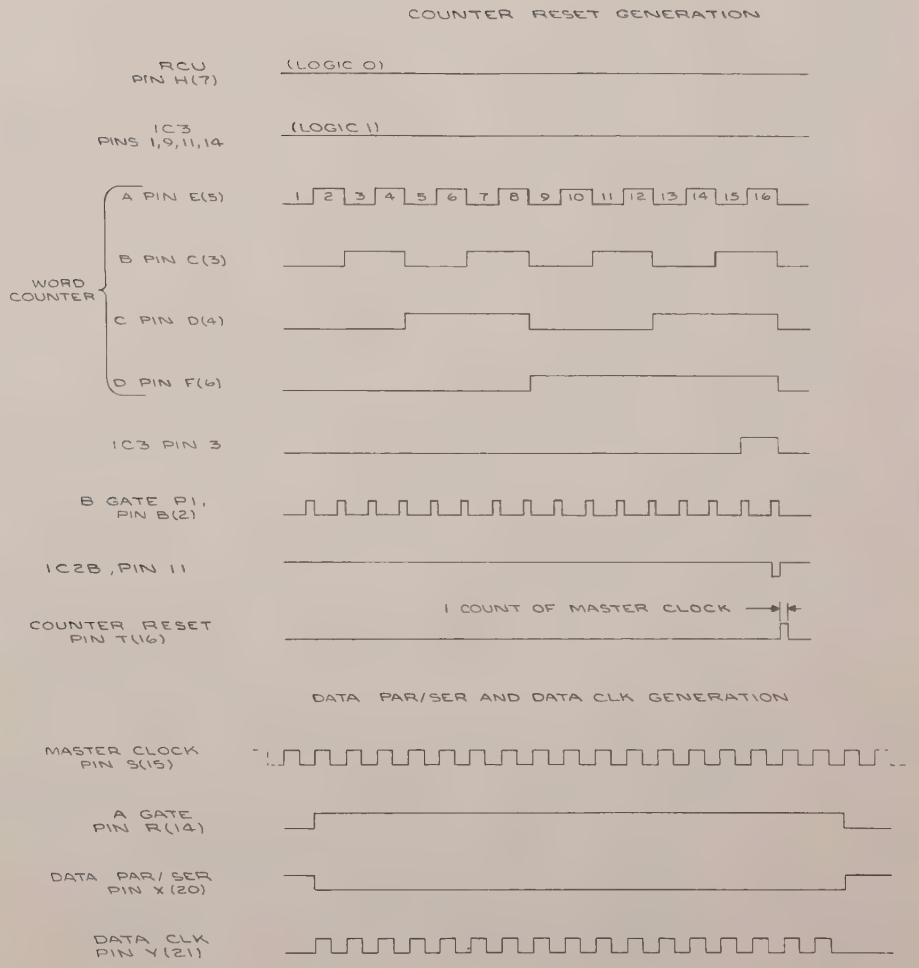


FIGURE 6-11
WAVEFORMS
BOARD 9055
TRANSMIT WORD CONTROL
MODEL 2476

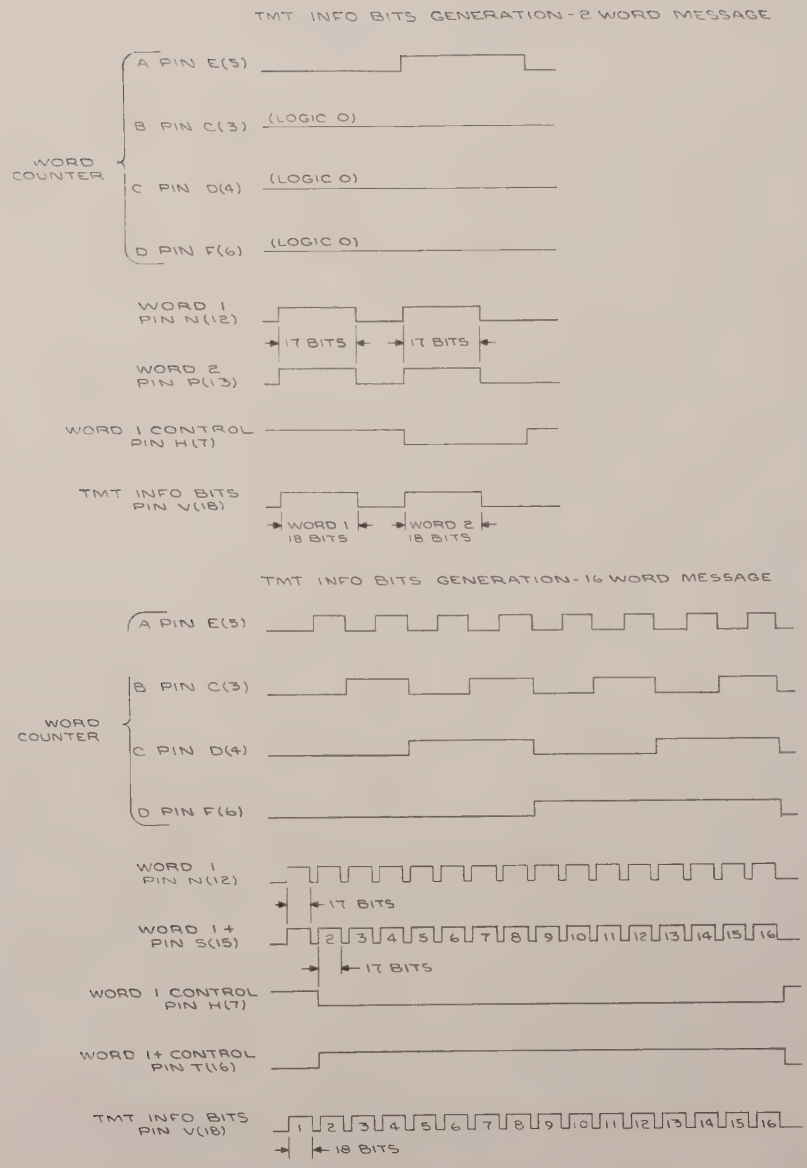

TMT INFO BITS GENERATION - 2 WORD MESSAGE
WORD COUNTER
A PIN E(5)
B PIN C(3)
(LOGIC 0)
C PIN D(4)
(LOGIC 0)
D PIN F(6)
(LOGIC 0)
WORD 1 PIN N(12)
17 BITS
17 BITS
WORD 2 PIN P(13)
WORD 1 CONTROL PIN H(7)
TMT INFO BITS PIN V(18)
WORD 1 18 BITS
WORD 2 18 BITS
TMT INFO BITS GENERATION - 16 WORD MESSAGE
WORD COUNTER
A PIN E(5)
B PIN C(3)
C PIN D(4)
D PIN F(6)
WORD 1 PIN N(12)
17 BITS
WORD 1+ PIN S(15)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
17 BITS
WORD 1 CONTROL PIN H(7)
WORD 1+ CONTROL PIN T(16)
TMT INFO BITS PIN V(18)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
18 BITS

FIGURE 6-12
WAVEFORMS
BOARD 9056
TRANSMIT WORD SELECTOR
MODEL 2476

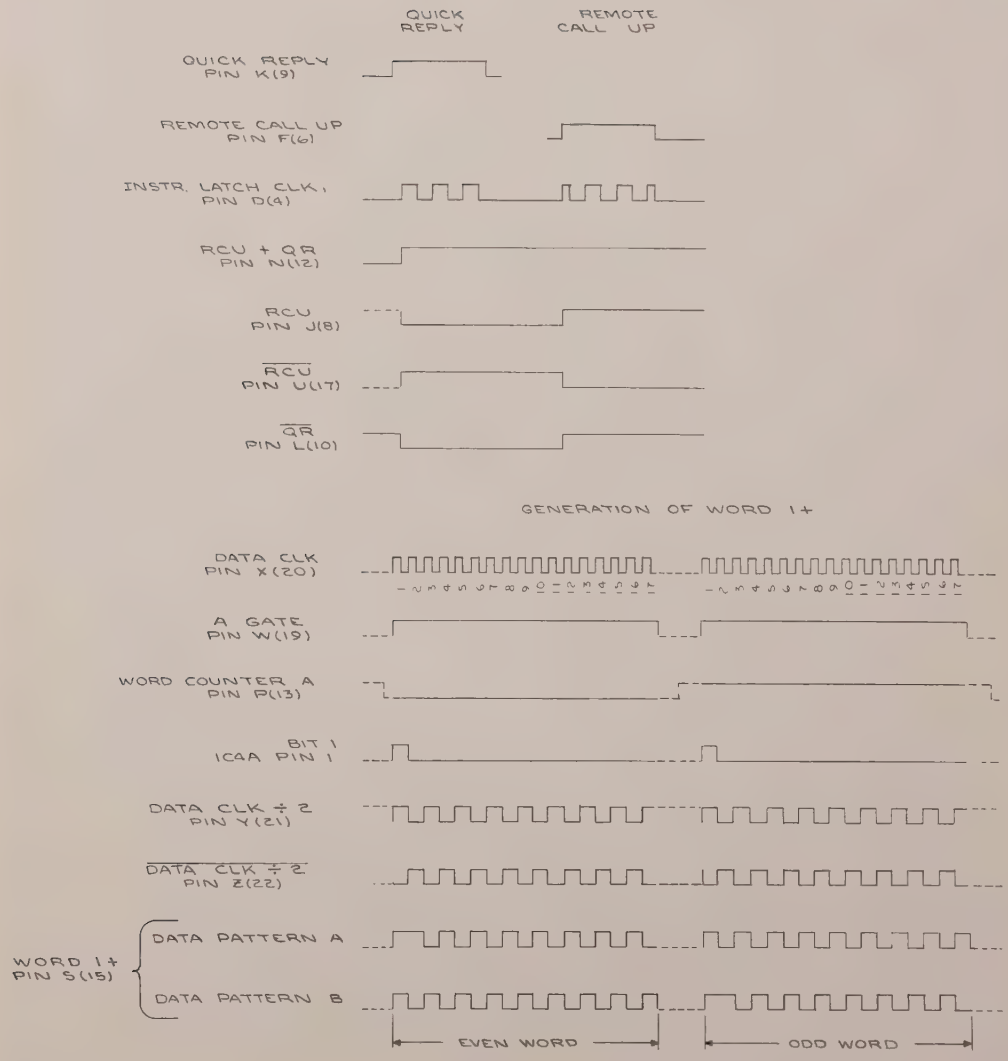


FIGURE 6-13
WAVEFORMS
BOARD 9057
INSTRUCTION CONTROL LOGIC II
MODEL 2476

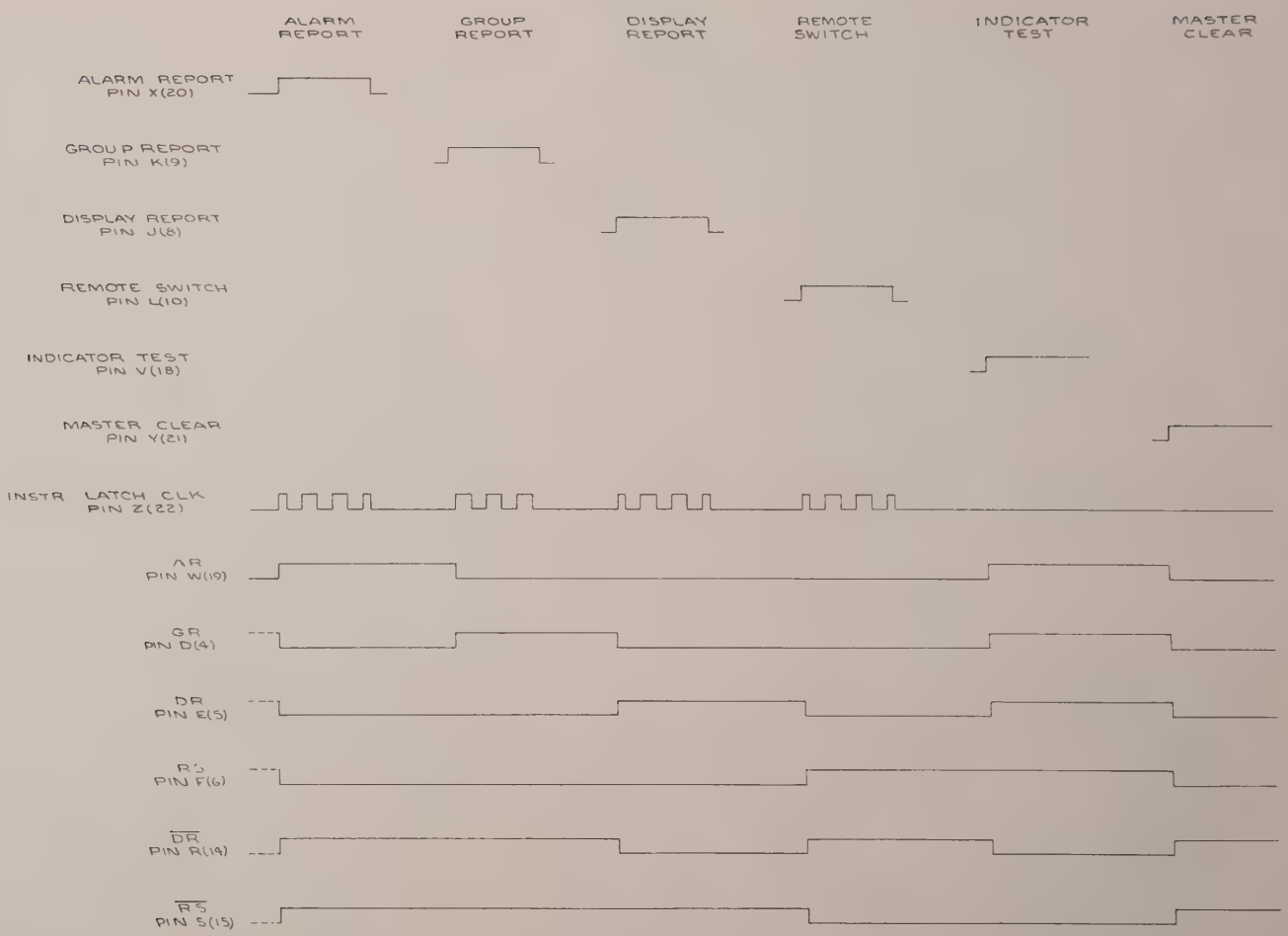


FIGURE 6-14
WAVEFORMS
BOARD 9051
INSTRUCTION CONTROL LOGIC I
MODEL 2475

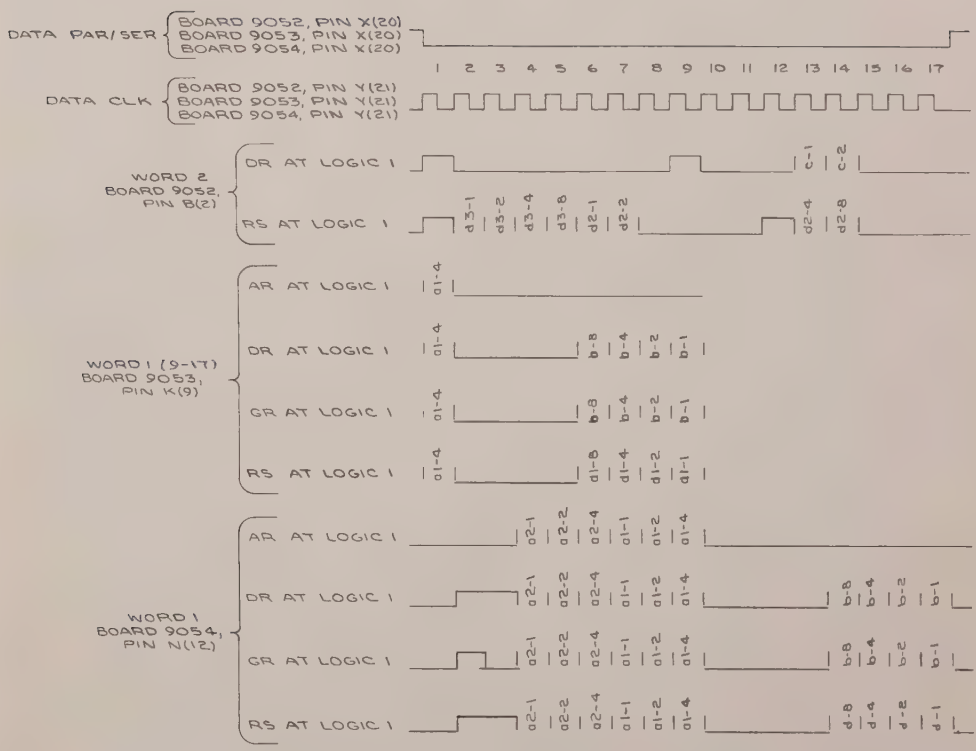


FIGURE 6-15
WAVEFORMS
BOARDS 9052, 9053, 9054
WORD REGISTERS
MODEL 2475

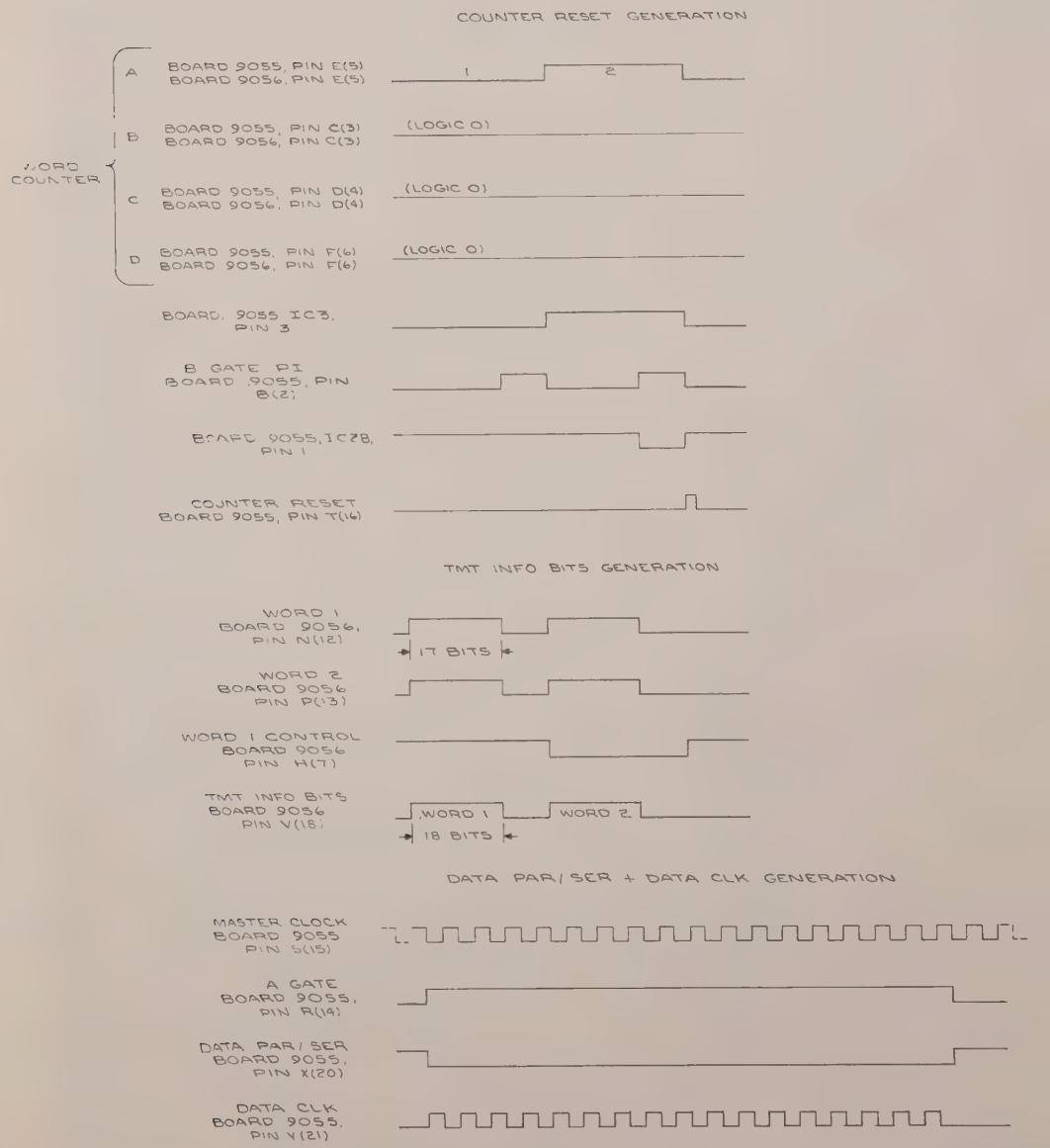


FIGURE 6-16
WAVEFORMS
BOARDS 9055, 9056
TRANSMIT WORD CONTROL, SELECTOR
MODEL 2475

WORD 1, 2, 3, 4, GENERATION

BIT SWITCHES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
WORD 1	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1
WORD 2	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
WORD 3	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0
WORD 4	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0

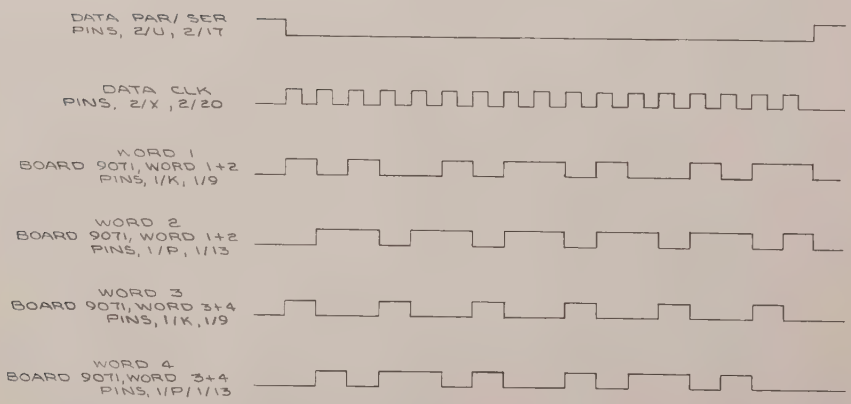


FIGURE 6-17
WAVEFORMS
BOARD 9071
WORD 1 AND 2 REGISTER
WORD 3 AND 4 REGISTER
MODEL 2477

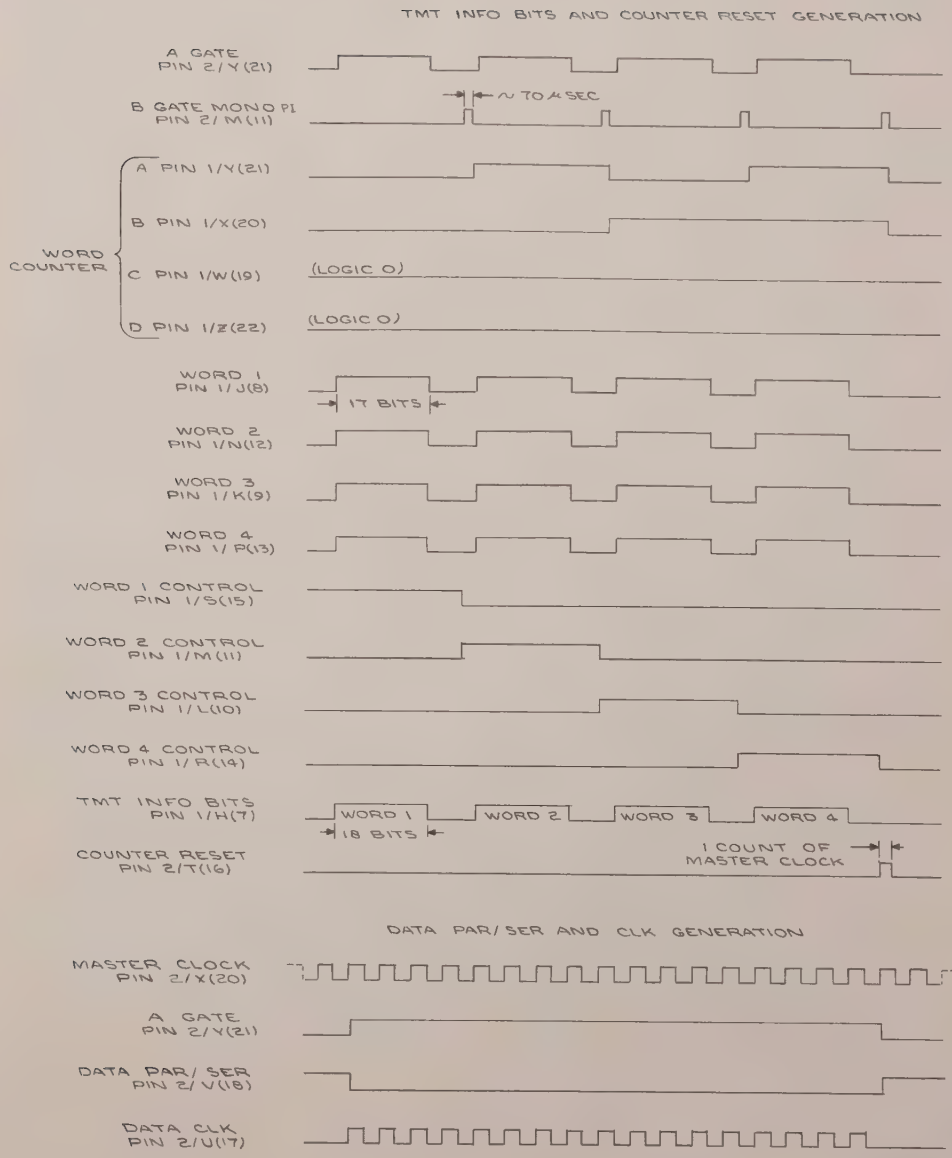


FIGURE 6-18
WAVEFORMS
BOARD 9073
TRANSMIT WORD SELECTOR AND CONTROL
MODEL 2477

Parts List and Circuit Diagrams

7-1. SCOPE OF THIS SECTION

7-1a. Most of the information normally required for troubleshooting and repairing the E-TELEMETRY STATION TEST SET (BTS and PI units) is included in this section

7-1b. The information provided includes:

Board Locations
Component Locations
Rear Connector schematics indicating lug functions
Schematic Diagrams, Board Component Locations and Replaceable Parts Lists
Semi-conductor and Integrated Circuit Legends
Printed Circuit Board lug identification

7-2 SCHEMATIC DIAGRAMS

7-2a. Figures 7-3 through 7-15 on the following pages contain the schematic diagrams, parts lists and component locations for the Model 2474 BTS. Like-wise Figures 7-16 through 7-24 contain the diagrams for the Model 2476 PI Figures 7-25 through 7-32 contain those for the Model 2475 PI and Figures 7-33 through 7-38 pertain to the Model 2477. Figures 7-39 through 7-43 contain the diagrams for available test cables namely E1/E2 Test Cable, E2A Test Cable, TCT Test Cable and the interconnecting cable. The schematic diagrams are included in this section as foldouts for convenience when reviewing Section 3 or Troubleshooting as per Section 6 instructions.

7-2b. Unless otherwise specified, all resistance and capacitance values shown on the schematics are:

Resistance in "ohms"
Capacitance in "microfarads"
All ± 1% resistors have 1/8 watt ratings
All other resistors have 1/4 watt ratings

7-2c. The schematic diagrams contain the following symbols:

K — 1000
pF — Picofarads
⊘ — Screwdriver adjustment
* — Factory selected component
START — Border indicates front panel control

7-2d. All drawings, lists and diagrams, pertaining to a particular module are grouped in the following manner:

Model 2474 (BTS) DRAWINGS, LISTS and DIAGRAMS
Model 2476 (PI) DRAWINGS, LISTS AND DIAGRAMS
Model 2475 (PI) DRAWINGS, LISTS and DIAGRAMS
Model 2477 (PI) DRAWINGS, LISTS and DIAGRAMS

7-3. COMPONENT LOCATIONS

7-3a. The board component layout drawings are located to the left of each corresponding schematic diagram. The component side as well as the foil side of the printed circuit (P.C.) board are illustrated. Their purpose is to aid one in locating a physical component referenced to schematic symbols.

7-3b. All components not mounted on P. C. boards are located on the COMPONENT AND PRINTED CIRCUIT BOARD LOCATIONS — FIGURES 7-3, 7-16, 7-25 and 7-33.

7-4. REPLACEABLE PARTS LISTS

7-4a. Tables identifying the replaceable electronic components are located on all drawings in this section except Figures 7-1, 7-2, 7-4, 7-5, 7-17, 7-26 and 7-34.

7-5. SEMI-CONDUCTOR LEGEND (TABLE 7-1)

7-5a. Changes and improvements in the semi-conductor products available for commercial use necessitates type changes from time to time. To eliminate confusion and costly paperwork, many of these changes will be covered in the following legend. The purpose of this legend is to acknowledge the fact that the type number on a semi-conductor found in a piece of equipment will not necessarily correspond with the type number given on the schematic diagram.

7-5b. The legend is not intended to be an interchangeability list although in many cases good quality components within a given category may be substituted with acceptable results. Normally, replacements should be made using components having the same type number as the component being replaced.

7-5c. Those components bearing an asterisk on the schematic diagram are factory selected components and should be obtained from Quan-Tech.

7-5d. It should be noted that the incoming inspection procedure followed by Quan-Tech includes noise screening on most semi-conductors.

7-6. INTEGRATED CIRCUIT LEGEND (TABLE 7-2)

7-6a. The I. C. LEGEND is intended to give the reader some insight as to the internal functions of each I. C. used in this equipment and the function of each pin of the I. C.

7-6b. Illustrated in the I. C. LEGEND are the 28 different I. C's incorporated including OP AMPS, COUNTERS, BUFFERS, FLIP-FLOPS, SHIFT REGISTERS, LATCHES, etc.

7-7. PRINTED CIRCUIT BOARD LUG IDENTIFICATION

7-7a. Figure 7-1 (b) illustrates the identification and orientation of a printed circuit board and connector having 22 pins.

7-7b. When a P. C. Board having copper on one side only is used, its pin identification is indicated in Figure 7-1 (a) and (b), its schematic references are A(1), B(2), C(3) etc. The copper side faces the observer when viewed as shown in Figure 7-1 (a).

7-7c. When a P. C. Board having copper on both sides is used its pin orientation is indicated in Figure 7-1 (c) and its schematic references shall be as follows:

1a) A, B, C etc. signifies that electrical connections are made to lettered side of P. C. Board ("A" side).

2b) 1, 2, 3 etc. signifies that electrical connections are made to numbered side of P. C. Board ("1" side).

7-7d. In the Model 2477, both single sided and double sided copper P. C. Boards incorporate 2 connectors per board. The same basic rules apply as above except for identification of the connectors. See Figure 7-2.

7-8. REAR CONNECTOR SCHEMATICS

7-8a. The rear connector schematics are included to identify the function of each signal leaving or entering each unit via the rear connector pins. Refer to FIGURES 7-4, 7-5, 7-17, 7-26 and 7-34.

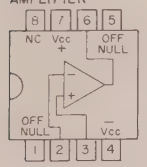
TABLE 7-1
SEMI-CONDUCTOR LEGEND

TYPE NO. ON SCHEMATIC	TYPE NO. IN EQUIPMENT	TYPE NO. ON SCHEMATIC	TYPE NO. IN EQUIPMENT
1N3208	1N3208, 1N3210	MJ3000	MJ3000
1N914B	1N914B, 1N4151 1N415B	2N3643	2N3643, 2N2219, A322, 2N929
1N276	1N276, 1N69	2N3644	2N3250, 2N3251
1N482	1N482, 1N3604, 1N3605	TIS59	TIS73, 2N3819, TIS75
1N757	1N757	78MO5	78MO5
1N968	1N968	78MO8	78MO8
MV-5054-3	MV-5054-3		
1N4151	1N4151, 1N415B, 1N914B		

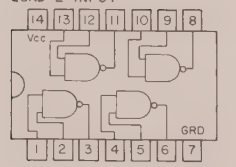
(TOP VIEW)

(TOP VIEW)

72741P
OPERATIONAL AMPLIFIER



74L00
NAND GATES
QUAD 2 INPUT



74L02
NOR GATES
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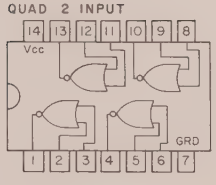
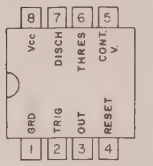


NE555V
TIMER



CD4001A
NOR GATES
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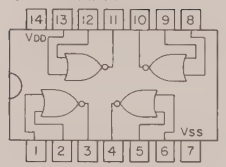
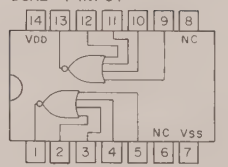
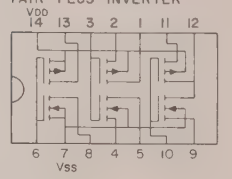


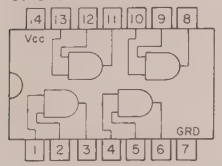
CD4002A
NOR GATES
DUAL 4 INPUT



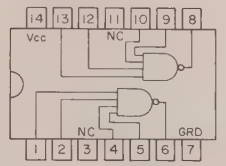
CD4007A
DUAL COMPLEMENTARY PAIR PLUS INVERTER



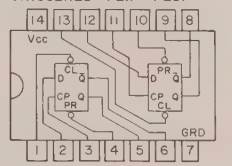
74LS08
AND GATES
QUAD 2 INPUT



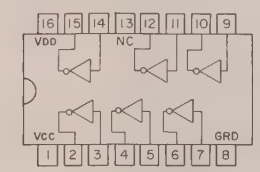
74L20
NAND GATES
DUAL 4 INPUT



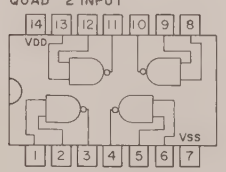
7474
DUAL D TYPE EDGE-TRIGGERED FLIP-FLOP



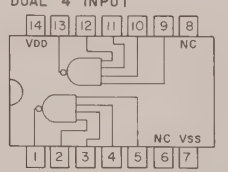
CD4009A
HEX BUFFER/CONVERTER



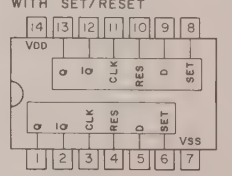
CD4011A
NAND GATES
QUAD 2 INPUT



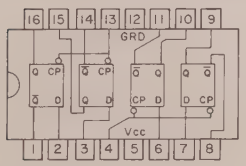
CD4012A
NAND GATES
DUAL 4 INPUT



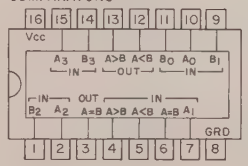
CD4013A
DUAL D TYPE FLIP-FLOP WITH SET/RESET



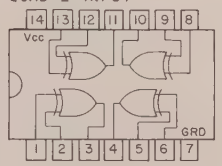
7475
QUADRUPLE BISTABLE LATCHES



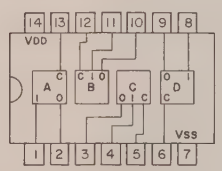
74L85
4-BIT MAGNITUDE COMPARATORS



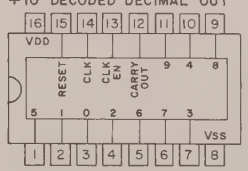
74L86
EXCLUSIVE-OR GATES
QUAD 2 INPUT



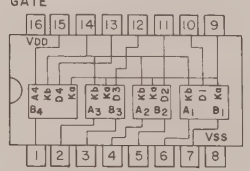
CD4016A
QUAD BILATERAL SWITCH



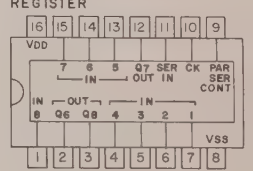
CD4017A
DECADE COUNTER / DIVIDER +10 DECODED DECIMAL OUT



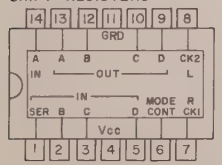
CD4019A
QUAD AND-OR SELECT GATE



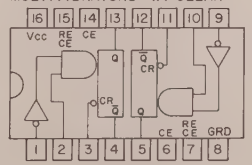
CD4021A
8 STAGE STATIC SHIFT REGISTER



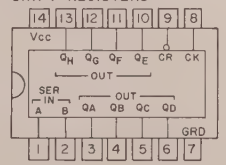
74L95
4-BIT RIGHT/LEFT SHIFT REGISTERS



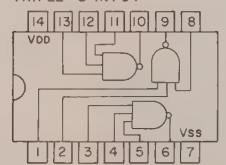
74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS W/CLEAR



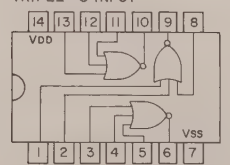
74L164
8-BIT PAR-OUT SERIAL SHIFT REGISTERS



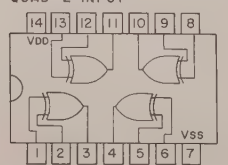
CD4023A
NAND GATES
TRIPLE 3 INPUT



CD4025A
NOR GATES
TRIPLE 3 INPUT



CD4030A
EXCLUSIVE-OR GATES
QUAD 2 INPUT



CD4040A
12 STAGE RIPPLE-CARRY BINARY COUNTER / DIVIDER

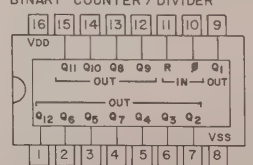


TABLE 7-2
INTEGRATED CIRCUIT LEGEND

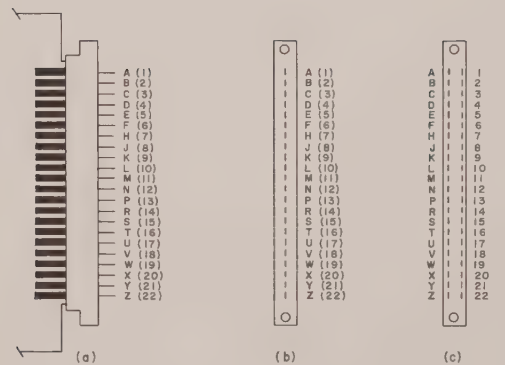
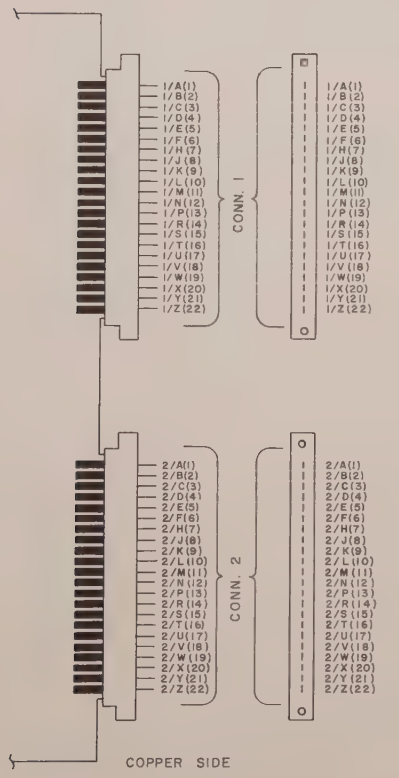
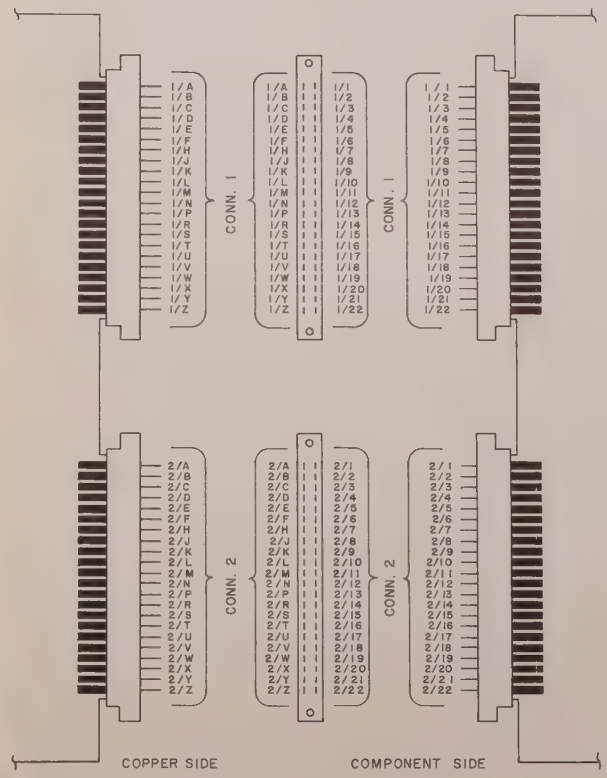


FIGURE 7-1
PRINTED CIRCUIT BOARD LUG IDENTIFICATION

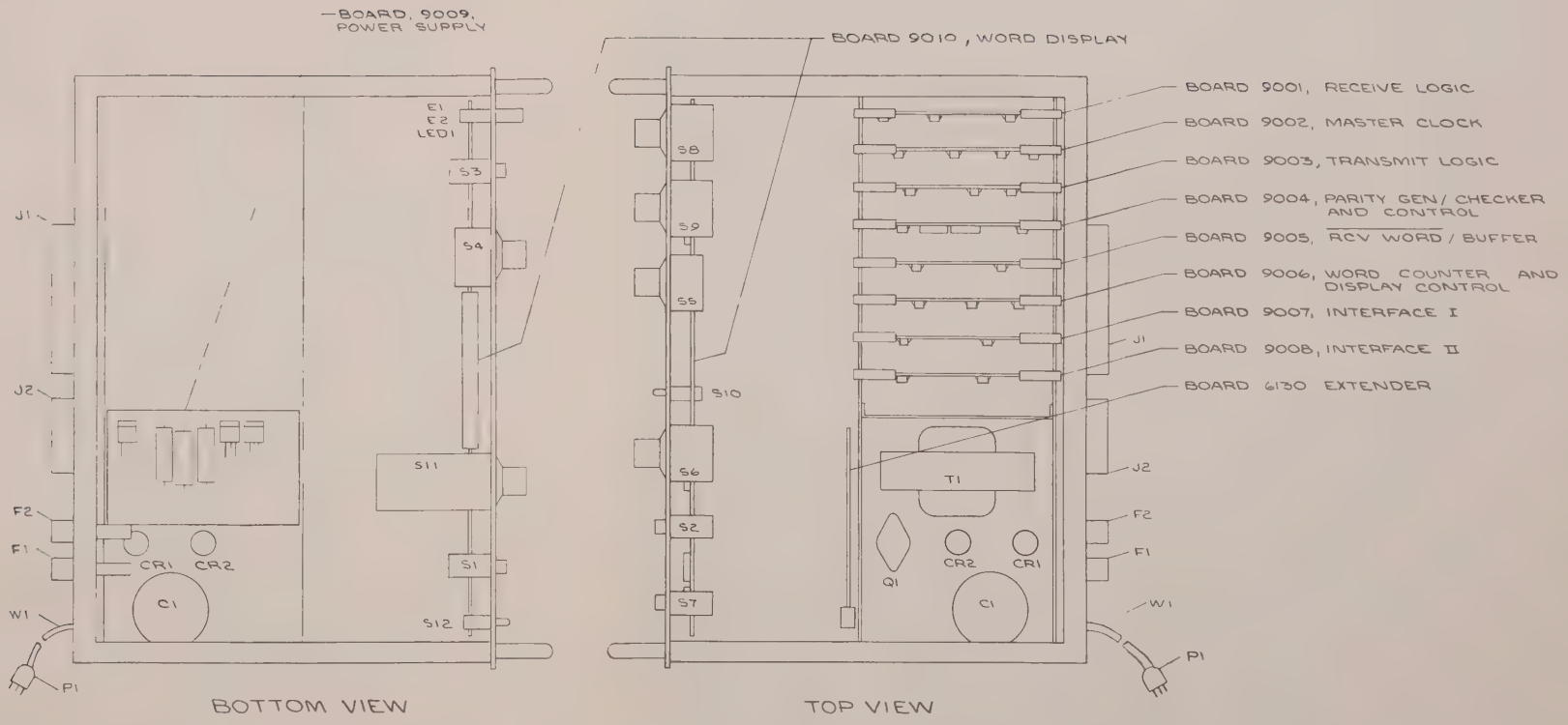


SINGLE SIDED COPPER P.C. BOARD



DOUBLE SIDED COPPER P.C. BOARD

FIGURE 7-2
PRINTED CIRCUIT BOARD LUG IDENTIFICATION
MODEL 2477



REPLACEABLE PARTS LIST

SYMBOL	DESCRIPTION
	Connector, Cinch Jones No.250-22-30-170 (9 Req'd)
C1	Capacitor, 12,000 mF, 25V, G. E. No.43F1964-CA3
CR1,CR2	Diode, 1N3208
E1	Post, Binding, E. F. Johnson No.111-102
E2	Post, Binding, E. F. Johnson No.111-103
F1,F2	Fuse, 3/4 A. Slow-Blow, Bussman Type MDL
J1	Connector, Amphenol No.26-4401-32P
J2	Connector, Amphenol No.26-4401-16P
LED1	Lamp, Monsanto No.MV-5054-3
P1	Part of W1
Q1	Transistor, MJ3000
S1-S3	Switch, Push Button, Grayhill No.4002
S4	Switch, Rotary, Quan-Tech No.3978
S5,S6	Switch, Rotary, Quan-Tech No.5198-3
S7	Switch, Push Button, Grayhill No.4002
S8,S9	Switch, Rotary, Quan-Tech No.5198-2
S10	Switch, Toggle, DPDT, Alco No.MST-215N
S11	Switch, Rotary, Quan-Tech No.6743
S12	Switch, Toggle, SPDT, C&K No.7101-SYCB
T1	Transformer, Stancor No.P-8357
W1	Line Cord (Includes P1), Belden No. 17409

FIGURE 7-3
COMPONENT AND PRINTED CIRCUIT BOARD LOCATIONS
MODEL 2474

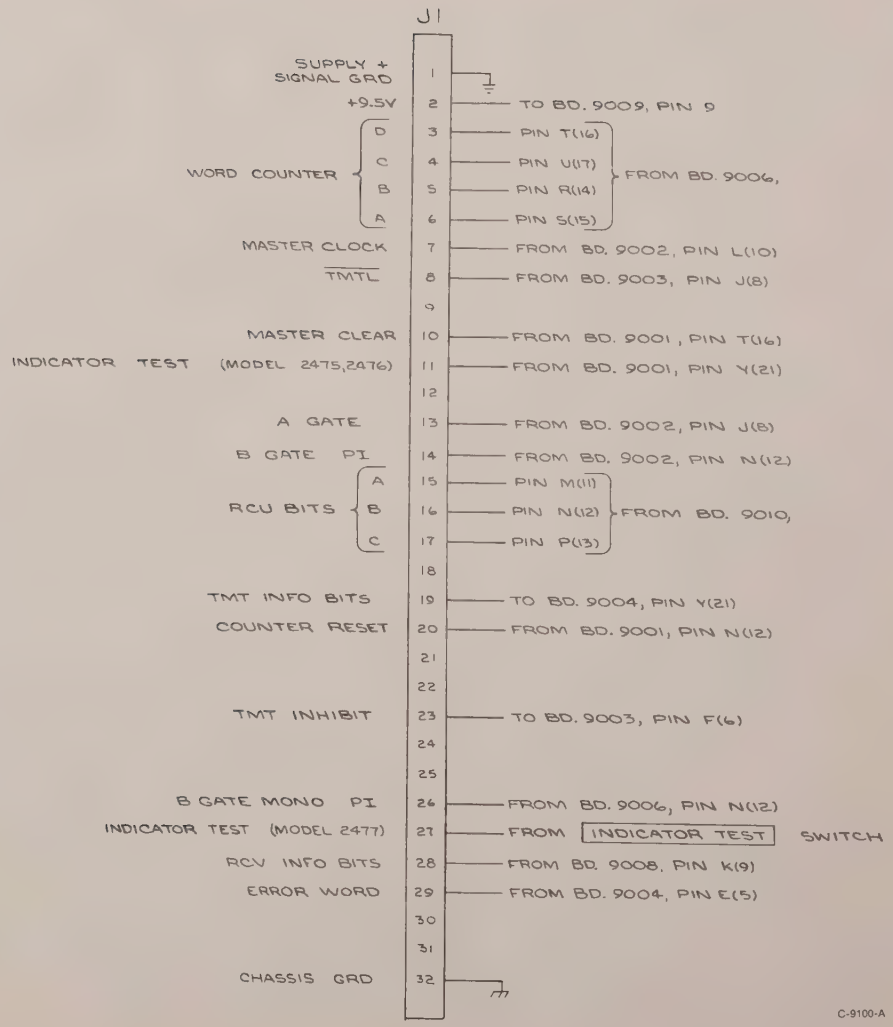


FIGURE 7-4
SCHEMATIC
CONNECTOR (BTS TO PI)
MODEL 2474

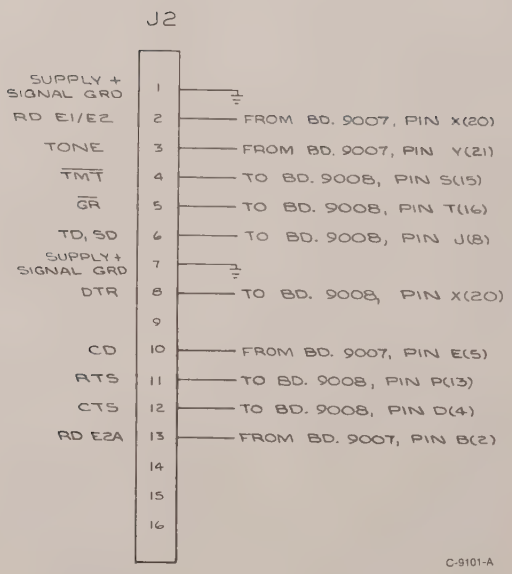
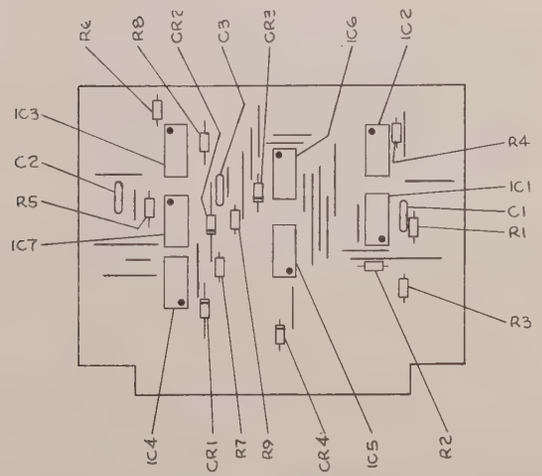
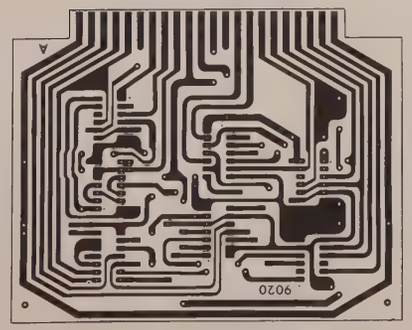


FIGURE 7-5
SCHEMATIC
CONNECTOR (BTS TO STATION)
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9001 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9020 Ejector, SAE No.6100 (2 Req'd)
C1-C3	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
CR1-CR4	Diode, 1N914B
IC1,IC2	Integrated Circuit, CD4013AE
IC3	Integrated Circuit, CD4001AE
IC4	Integrated Circuit, CD4013AE
IC5	Integrated Circuit, CD4001AE
IC6	Integrated Circuit, CD4030AE
IC7	Integrated Circuit, CD4001AE
R1	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, 4700 Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 10 Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R6,R7	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R8	Resistor, 27K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 150K Ohms, ±10%, 1/4W, A-B Type CB





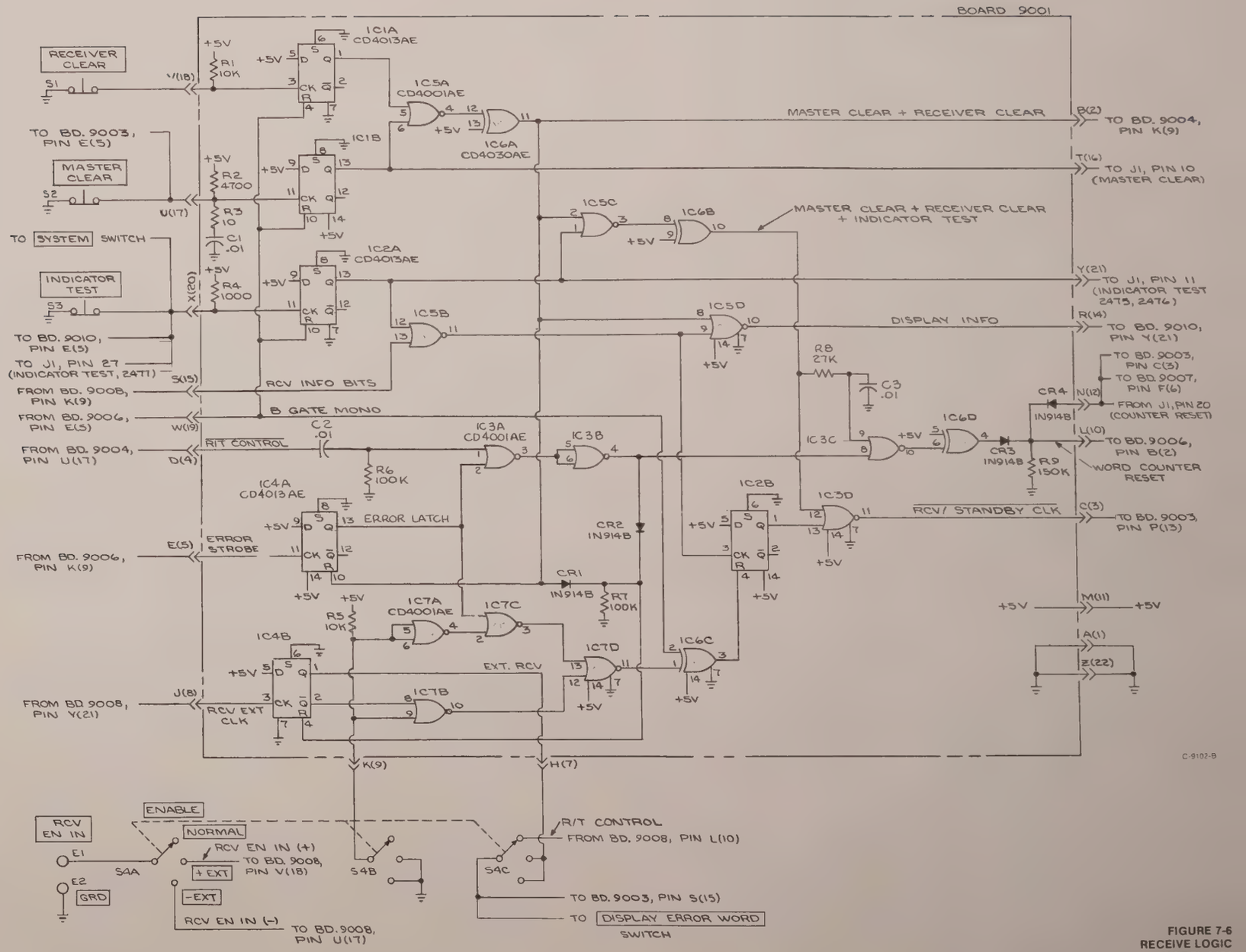
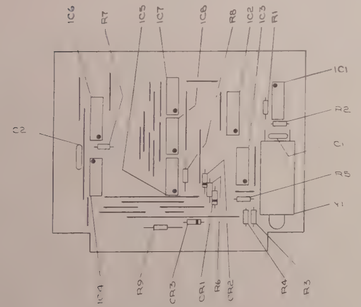
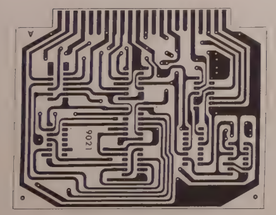


FIGURE 7-6
RECEIVE LOGIC
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASS'Y. 9002 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9021 Ejector, SAE No.6100 I2 Req'd
C1	Capacitor, 33 pF, ±10%, 1000V, Centralab No.DD-330
C2	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
CR1-CR3	Diode, 1N914B
IC1	Integrated Circuit, CD4007AE
IC2	Integrated Circuit, CD4040AE
IC3	Integrated Circuit, CD4016AE
IC4	Integrated Circuit, CD4030AE
IC5	Integrated Circuit, CD4013AE
IC6	Integrated Circuit, CD4017AE
IC7,IC8	Integrated Circuit, CD4013AE
R1	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, (Factory Selected), ±10%, ¼W, A-B Type CB
R3-R9	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
Y1	Crystal, 153.6 KHz, ±0.01%, 0.50°C, Series Mode, Bliley BH96W





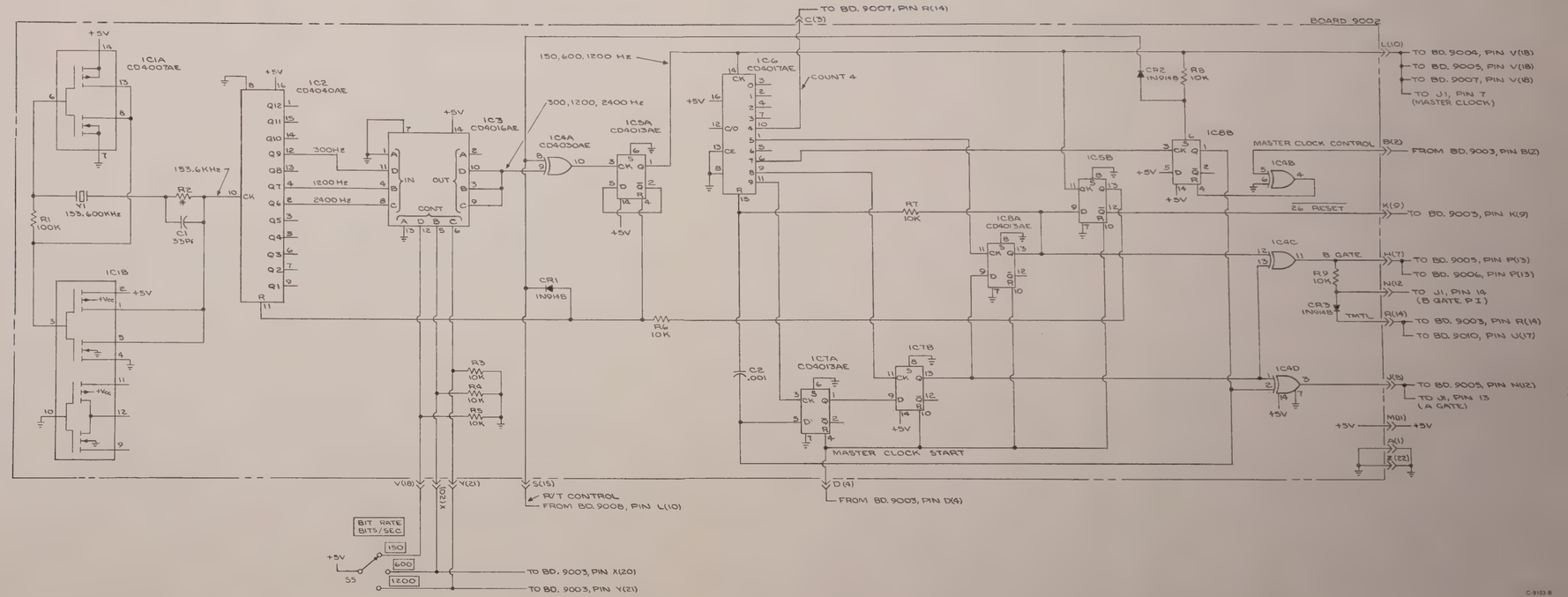
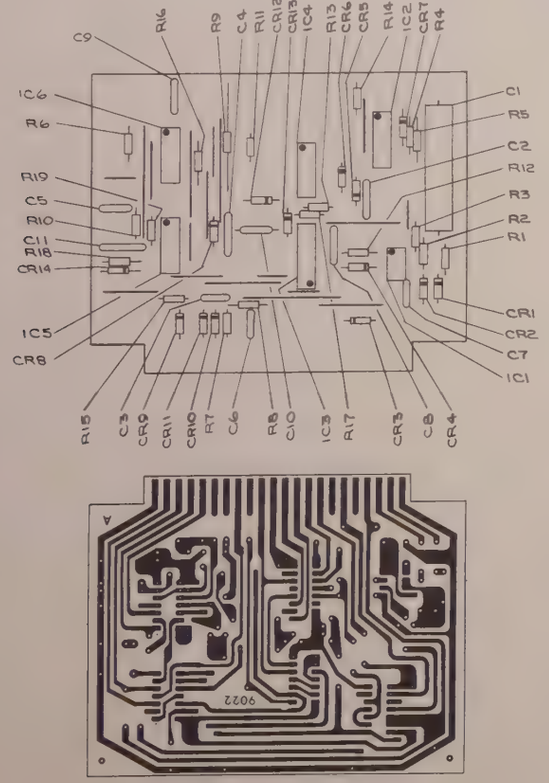


FIGURE 7-7
MASTER CLOCK
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9003 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9022
	Ejector, SAE No.6100, (2 Req'd)
C1	Capacitor, 3.3 mF, ±10%, 100V, ITT No.D1
C2	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C3	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C4	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C5	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C6	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C7	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C8	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C9,C10	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C11	Capacitor, 0.033mF, ±5%, 600V, Arco Type 1MD
CR1-CR14	Diode, 1N914B
IC1	Integrated Circuit, NE555V
IC2	Integrated Circuit, CD4001AE
IC3	Integrated Circuit, CD4009AE
IC4	Integrated Circuit, CD4001AE
IC5	Integrated Circuit, CD4013AE
IC6	Integrated Circuit, CD4001AE
R1 – R3	Resistor, (Factory Selected), ±10%, ¼W, A-B Type CB
R4	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R5,R6	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R7	Resistor, 10 Ohms, ±10%, 1/4W, A-B Type CB
R8	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R10	Resistor, 10 Ohms, ±10%, 1/4W, A-B Type CB
R11,R12	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R13	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R14,R15	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R16,R17	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R18	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R19	Resistor, 20K Ohms, ±1%, 1/8W, IRC No. CEA-TO



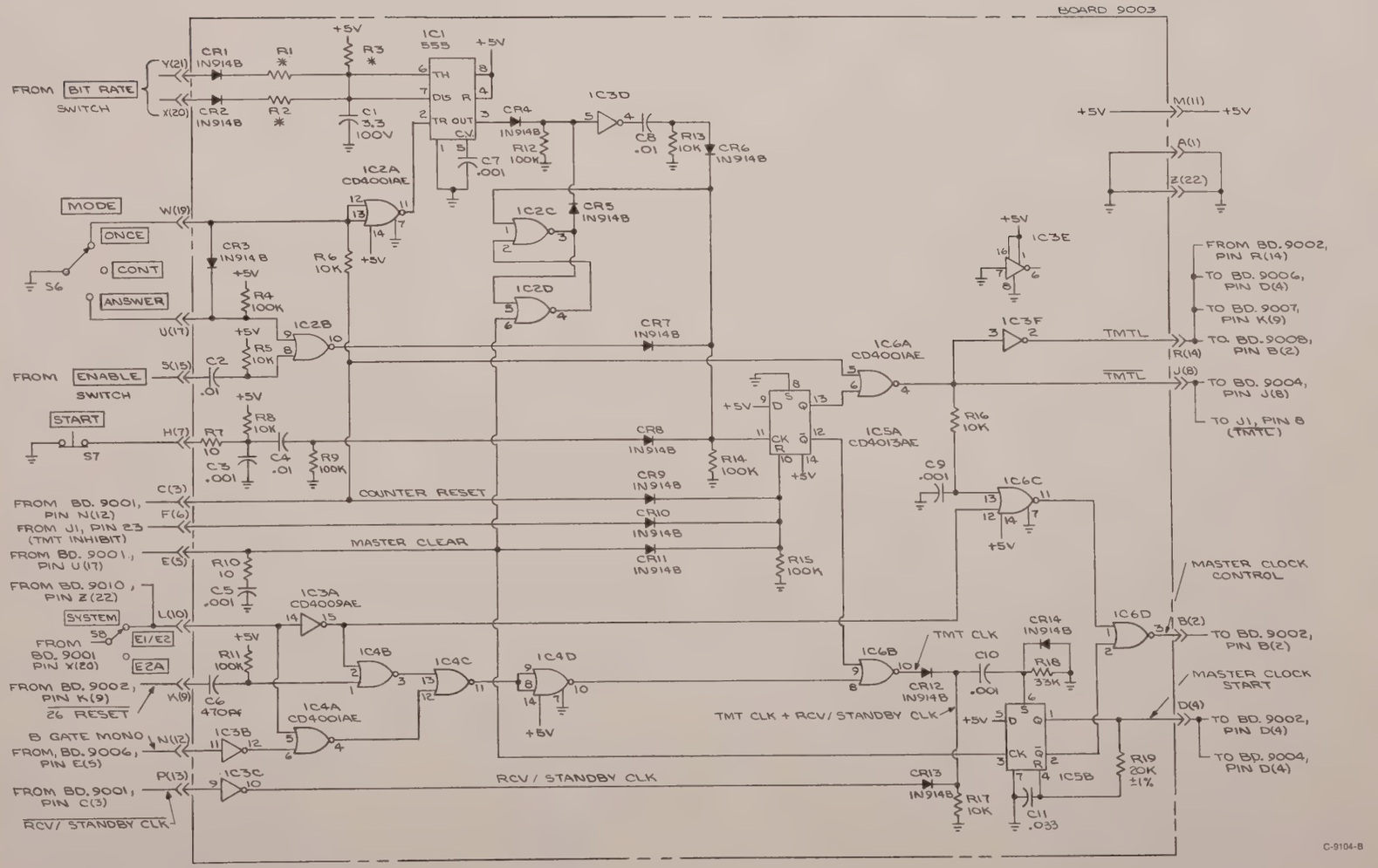
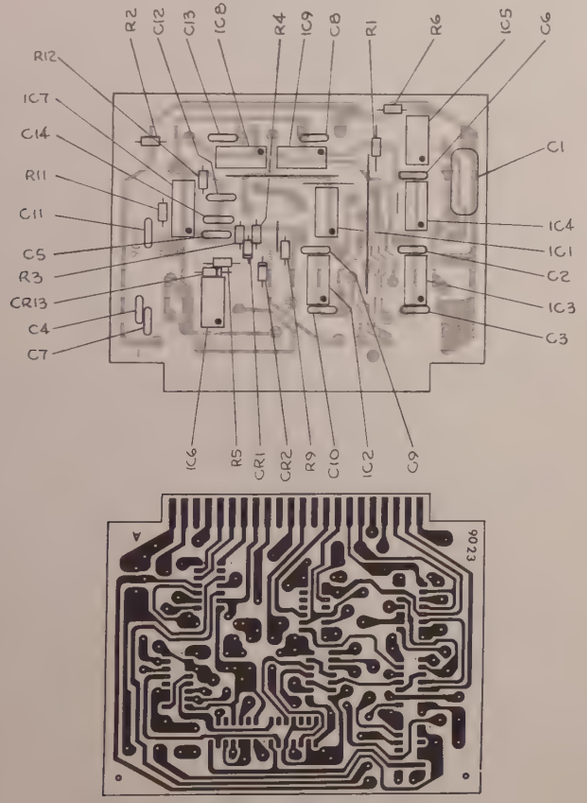


FIGURE 7-8
TRANSMIT LOGIC
MODEL 2474

REPLACEABLE PARTS LIST

QUAN-TECH ASSY. 9004 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan Tech No.9023 Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 0.0033 mF, ±5%, 600V, Arco No.MPD
C2,C3	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C4,C5	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C6	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C7	Capacitor, 0.001mF, ±20%, 1000V, Sprague No.5GA
C8-C11	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C12	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C13,C14	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
CR1-CR3	Diode, 1N914B
IC1	Integrated Circuit, 74L86N
IC2	Integrated Circuit, 74L00N
IC3	Integrated Circuit, 74LS08N
IC4	Integrated Circuit, 74L00N
IC5	Integrated Circuit, 74L20N
IC6	Integrated Circuit, CD4013AE
IC7	Integrated Circuit, 74123N
IC8,IC9	Integrated Circuit, 74L95N
R1	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, 22K Ohms, ±10%, 1/4 W, A-B Type CB
R3	Resistor, 470K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R7,R8	(Not used)
R9,R10	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R11, R12	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB



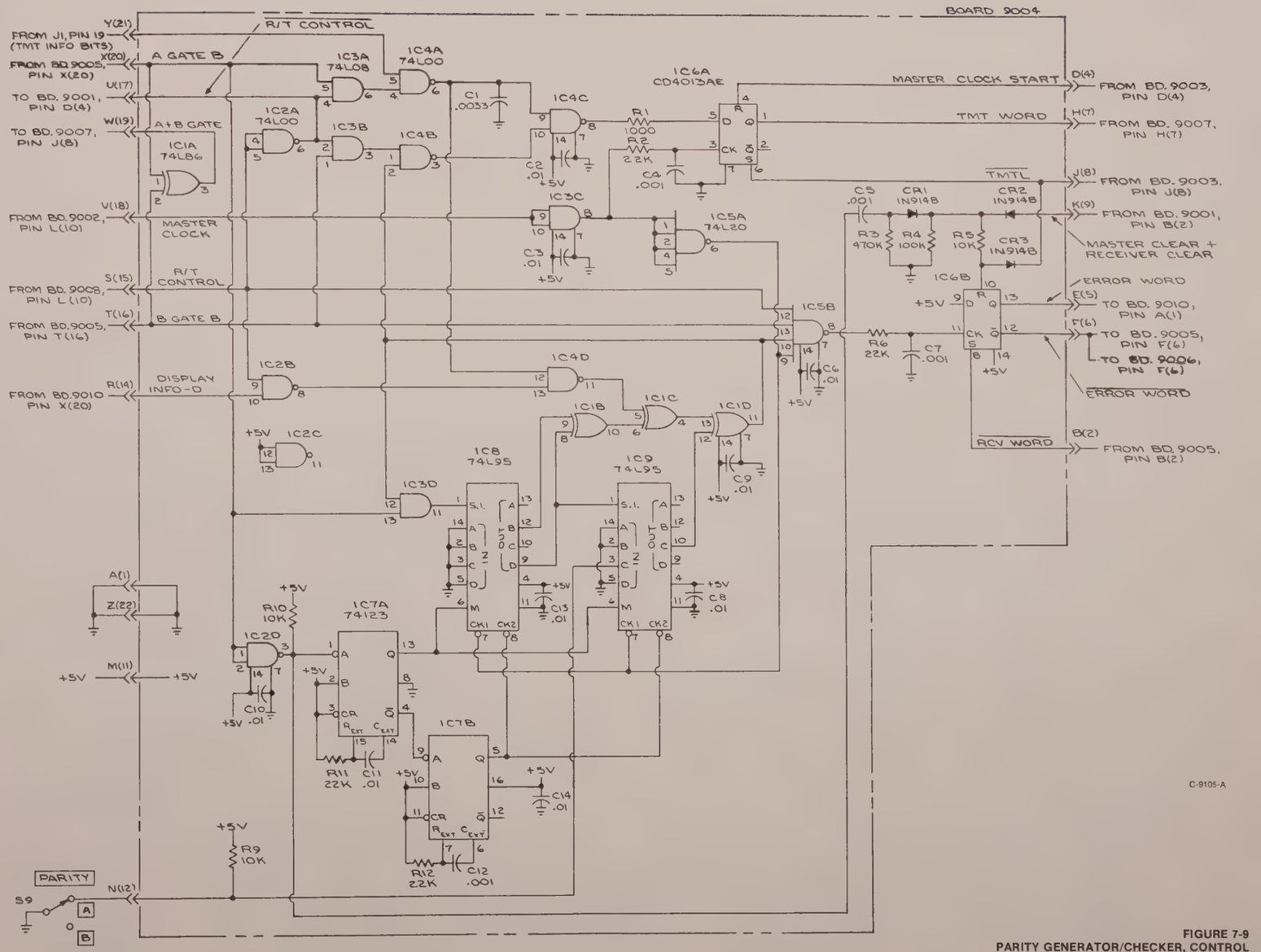
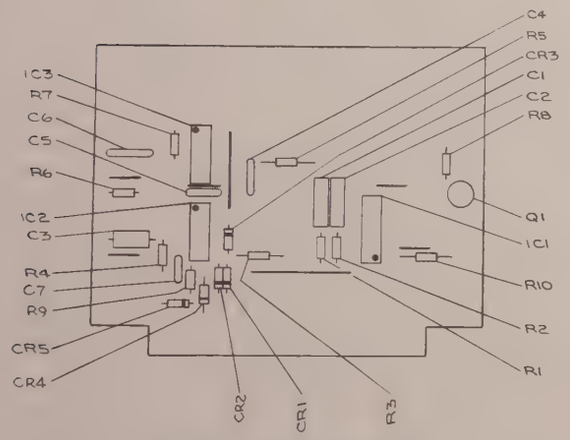
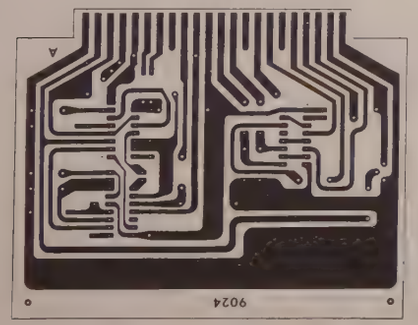


FIGURE 7-9
PARITY GENERATOR/CHECKER, CONTROL
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9005 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No 9024
	Ejector, SAE No.6100 (2 Req'd)
C1,C2	Capacitor, 1200 pF, ±5%, 500V, Arco No.DM20
C3	Capacitor, 0.1 mF, ±10%, 100V, ITT No.D1
C4-C6	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C7	Capacitor, 200 Pf, ± 10%, 1000V, Centralab No. DD-200
CR1-CR5	Diode, 1N914B
IC1	Integrated Circuit, CD4009AE
IC2	Integrated Circuit, CD4001AE
IC3	Integrated Circuit, CD4013AE
Q1	Transistor, 2N3643
R1,R2	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 220K Ohms, ±10%, 1/4W, A-B Type CB
R5-R7	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R8	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R10	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





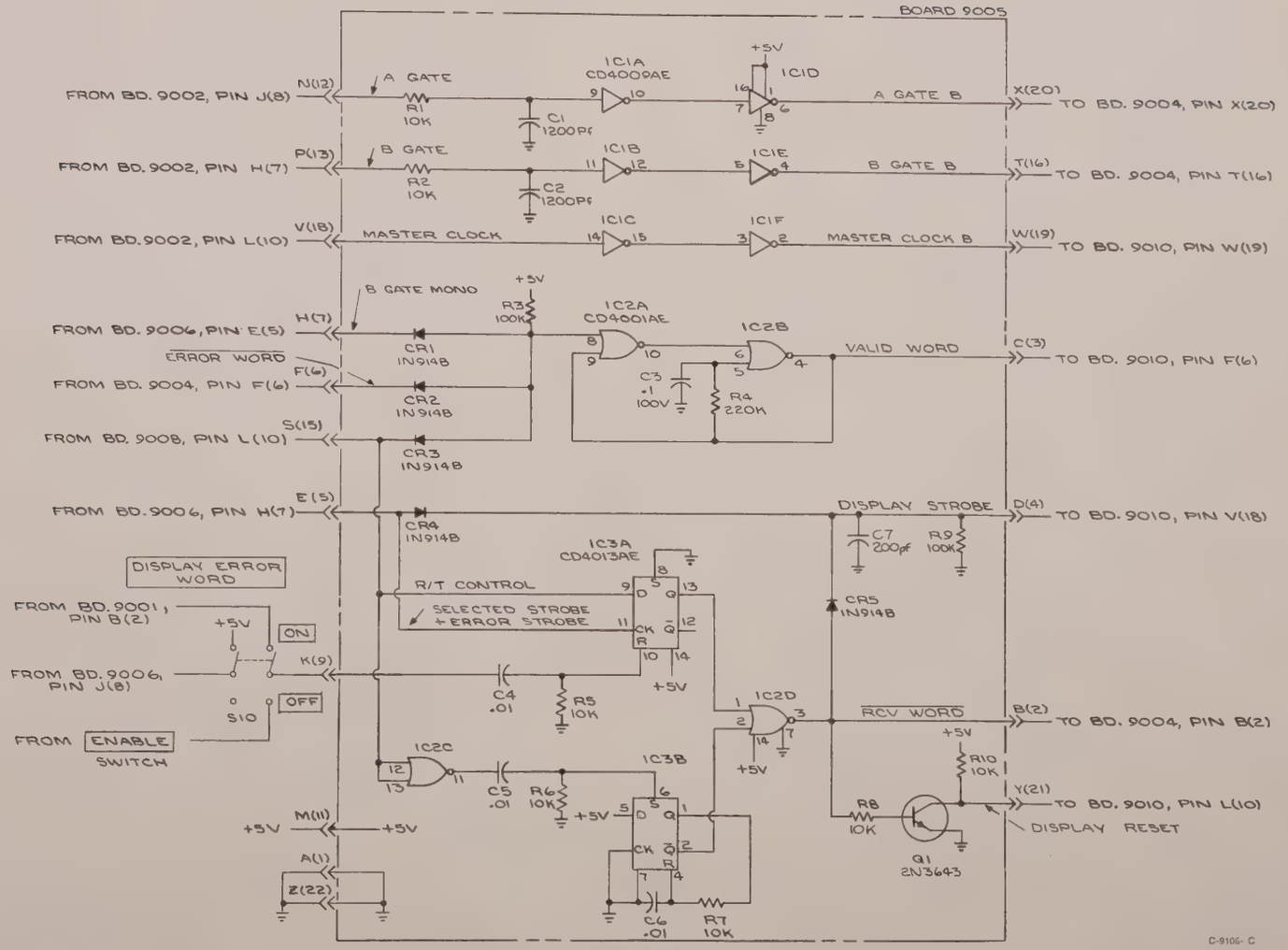
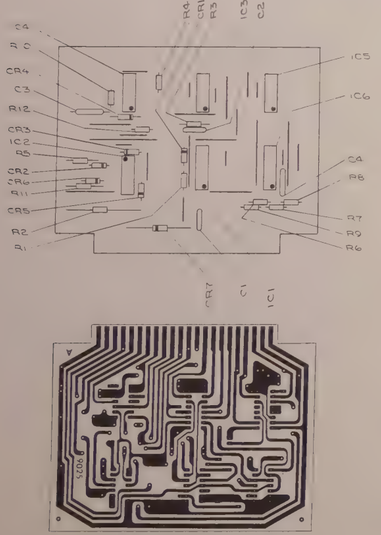


FIGURE 7-10
RCV WORD/BUFFER
MODEL 2474

REPLACEABLE PARTS LIST

QUAN-TECH ASSY. 9006 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9025
	Ejector, SAE No.6100 (2 Req'd)
C1-C3	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C4	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
CR1-CR7	Diode, 1N914B
IC1	Integrated Circuit, CD4009AE
IC2	Integrated Circuit, CD4001AE
IC3	Integrated Circuit, CD4013AE
IC4	Integrated Circuit, CD4001AE
IC5	Integrated Circuit, CD4013AE
IC6	Integrated Circuit, 74L85N
R1	Resistor, 68K Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 68K Ohms, ±10%, 1/4W, A-B Type CB
R4,R5	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R6-R9	Resistor, 4700 Ohms, ±10%, 1/4W, A-B Type CB
R10	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R11	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R12	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB



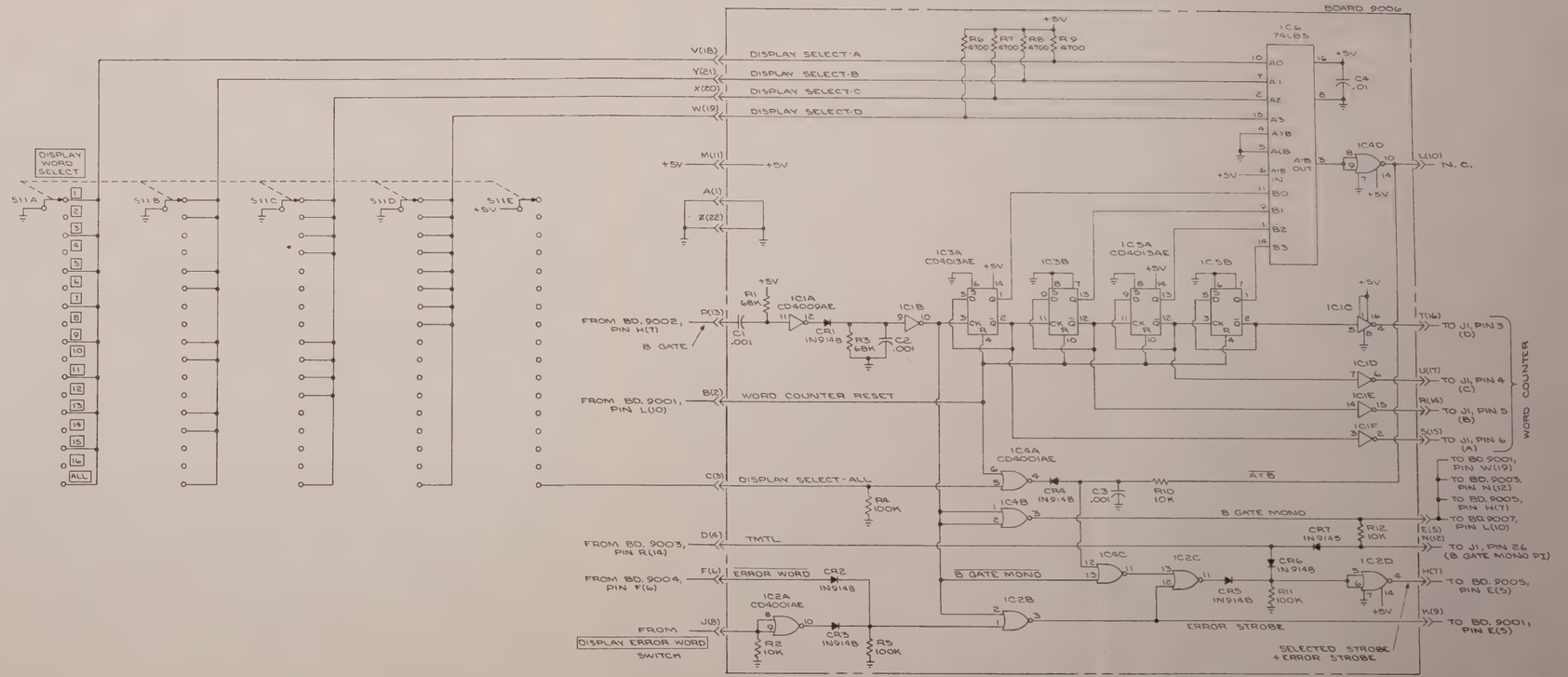
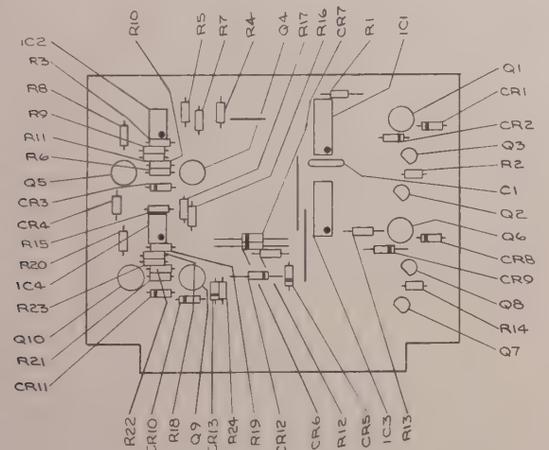
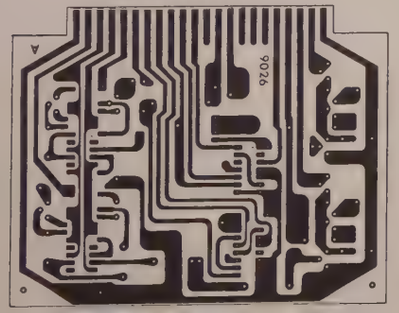


FIGURE 7-11
WORD COUNTER AND DISPLAY CONTROL
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9007 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9026
	Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
CR1-CR11	Diode, 1N914B
CR12, CR13	Diode, 1N276
IC1	Integrated Circuit, 74L02N
IC2	Integrated Circuit, 72741P
IC3	Integrated Circuit, CD4013AE
IC4	Integrated Circuit, 72741P
Q1	Transistor 2N3643
Q2	Transistor, Quan-Tech No. A-5657
Q3 & R2	Transistor, Resistor Matched Quan-Tech No. A-5658
Q4	Transistor, 2N3644
Q5, Q6	Transistor, 2N3643
Q7	Transistor, Quan-Tech No. A-5656
Q8 & R14	Transistor, Resistor Matched Quan-Tech No. A-5658
Q9	Transistor, 2N3644
Q10	Transistor, 2N3643
R1	Resistor, 3300 Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, (Factory Selected) Q3 & R2 Quan-Tech No. A-5658
R3	Resistor, 5600 Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R7,R8	Resistor, 82K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R10,R11	Resistor, 560 Ohms, ±10%, 1/4W, A-B Type CB
R12	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R13	Resistor, 3300 Ohms, ±10%, 1/4W, A-B Type CB
R14	Resistor, (Factory Selected) Q8 & R14 Quan-Tech No. A-5658
R15	Resistor, 5600 Ohms, ±10%, 1/4W, A-B Type CB
R16	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R17	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R18	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R19,R20	Resistor, 56K Ohms, ±10%, 1/4W, A-B Type CB
R21	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R22 R23	Resistor, 560 Ohms, ±10%, 1/4W, A-B Type CB
R24	Resistor, 10K Ohms, ±10%, ¼W, A-B Type CB





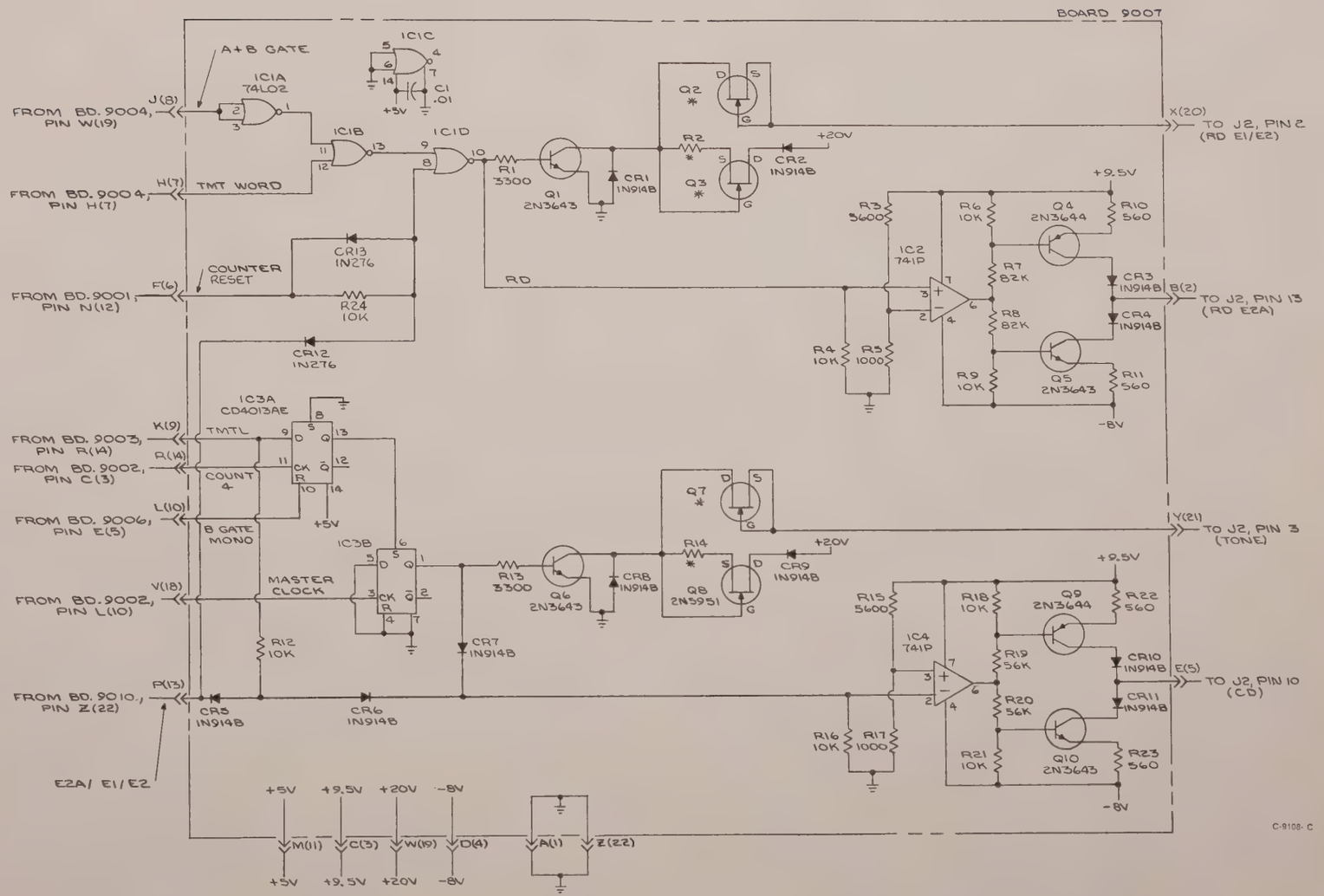
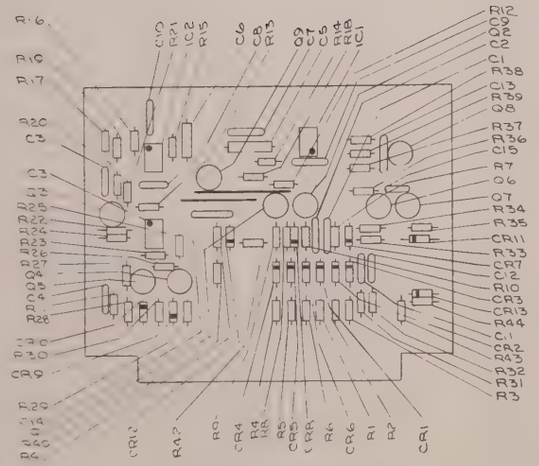


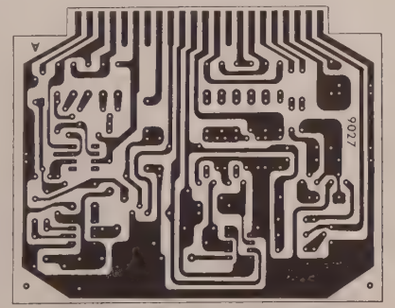
FIGURE 7-12
INTERFACE I
MODEL 2474

REPLACEABLE PARTS LIST

QUAN-TECH ASSY. 9008 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9027
	Ejector, SAE No.6100 (2 Req'd)
C1,C2	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C3,C4	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C5	Capacitor, 1 mF, ±5%, 100V, ITT No.D1
C6	Capacitor, 0.1 mF, ±10%, 100V, ITT No.D1
C7,C8	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C9,C10	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C11,C12	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C13,C14	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C15	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
CR1-CR10	Diode, 1N914B
CR11	Diode, 1N276
CR12,CR13	Diode, 1N914B
IC1,IC2	Integrated Circuit, NE555V
IC3	Integrated Circuit, 72741P
Q1-Q3	Transistor, 2N3643
Q4	Transistor, 2N3644
Q5	Transistor, 2N3643
Q6	Transistor, 2N3644
Q7-Q9	Transistor, 2N3643
R1-R6	Resistor, 3300 Ohms, ±10%, 1/4W, A-B Type CB
R7,R8	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R9,R10	Resistor, 470 Ohms, ±10%, 1/4W, A-B Type CB
R11	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R12	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R13	Resistor, 10K Ohms, ±10%,1/4W, A-B Type CB
R14	Resistor, 63K Ohms, ±1%, 1/8W, IRC No. CEA-TO
R15	Resistor, 120K Ohms, ±10%, 1/4W, A-B Type CB
R16	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R17	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R18,R19	Resistor, 2200 Ohms, ±10%, 1/4W, A-B Type CB
R20-R22	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R23	Resistor, 5600 Ohms, ±10%, 1/4W, A-B Type CB
R24	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R25	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R26,R27	Resistor, 82K Ohms, ±10%, 1/4W, A-B Type CB
R28	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R29,R30	Resistor, 560 Ohms, ±10%, 1/4W, A-B Type CB
R31-R33	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R34,R35	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R36	Resistor, 4700 Ohms, ±10%, 1/4W, A-B Type CB
R37	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R38	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
R39	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R40	Resistor, 3300 Ohms, ±10%, 1/4W, A-B Type CB
R41	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R42	Resistor, 4700 Ohms, ±10%, 1/4W, A-B Type CB
R43	Resistor, 3300 Ohms, ±10%, 1/4W, A-B Type CB
R44	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB





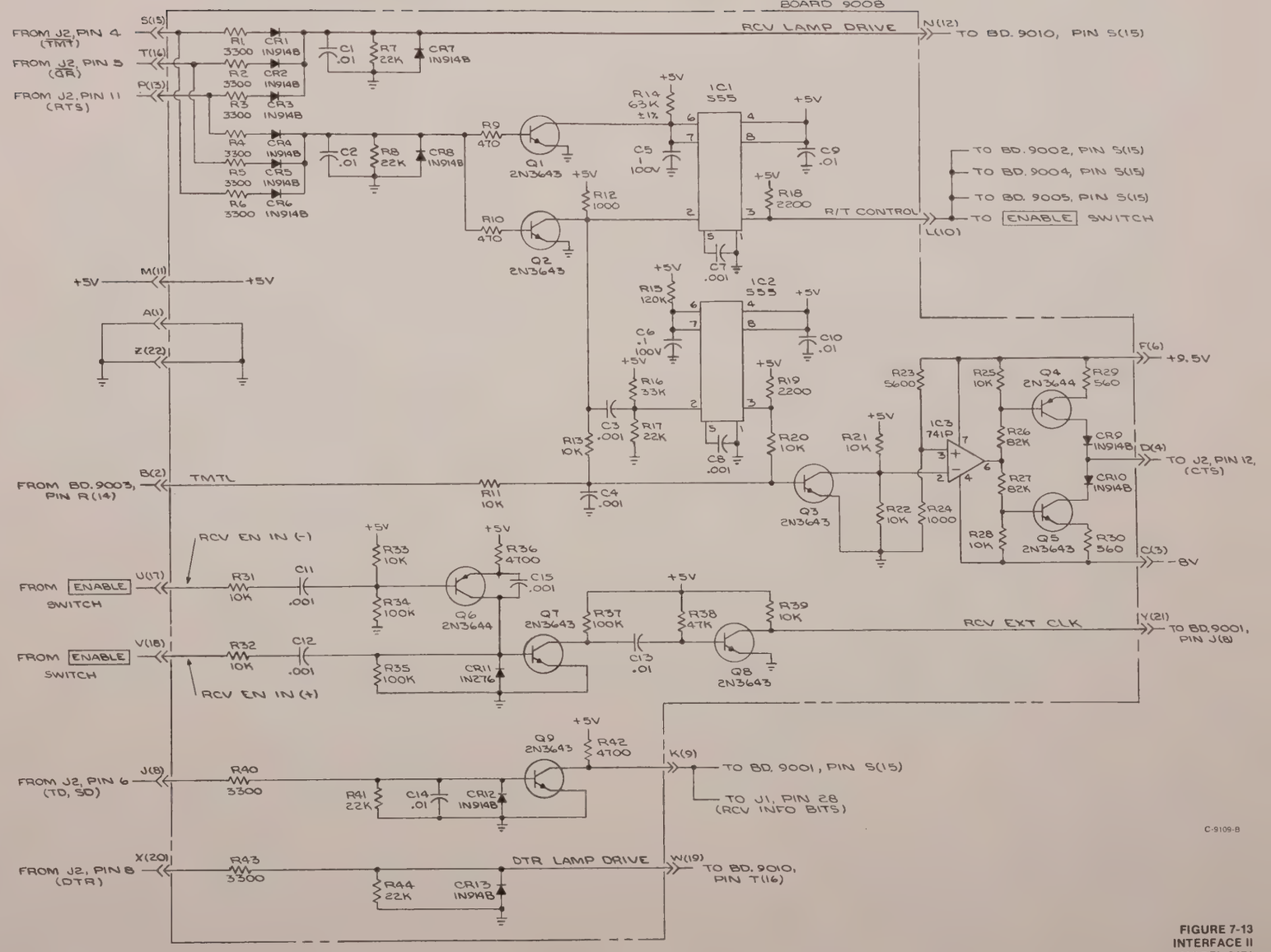
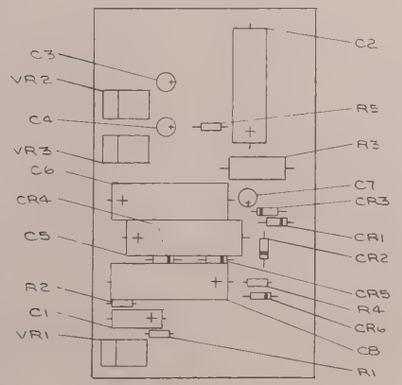
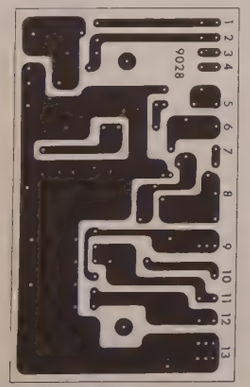


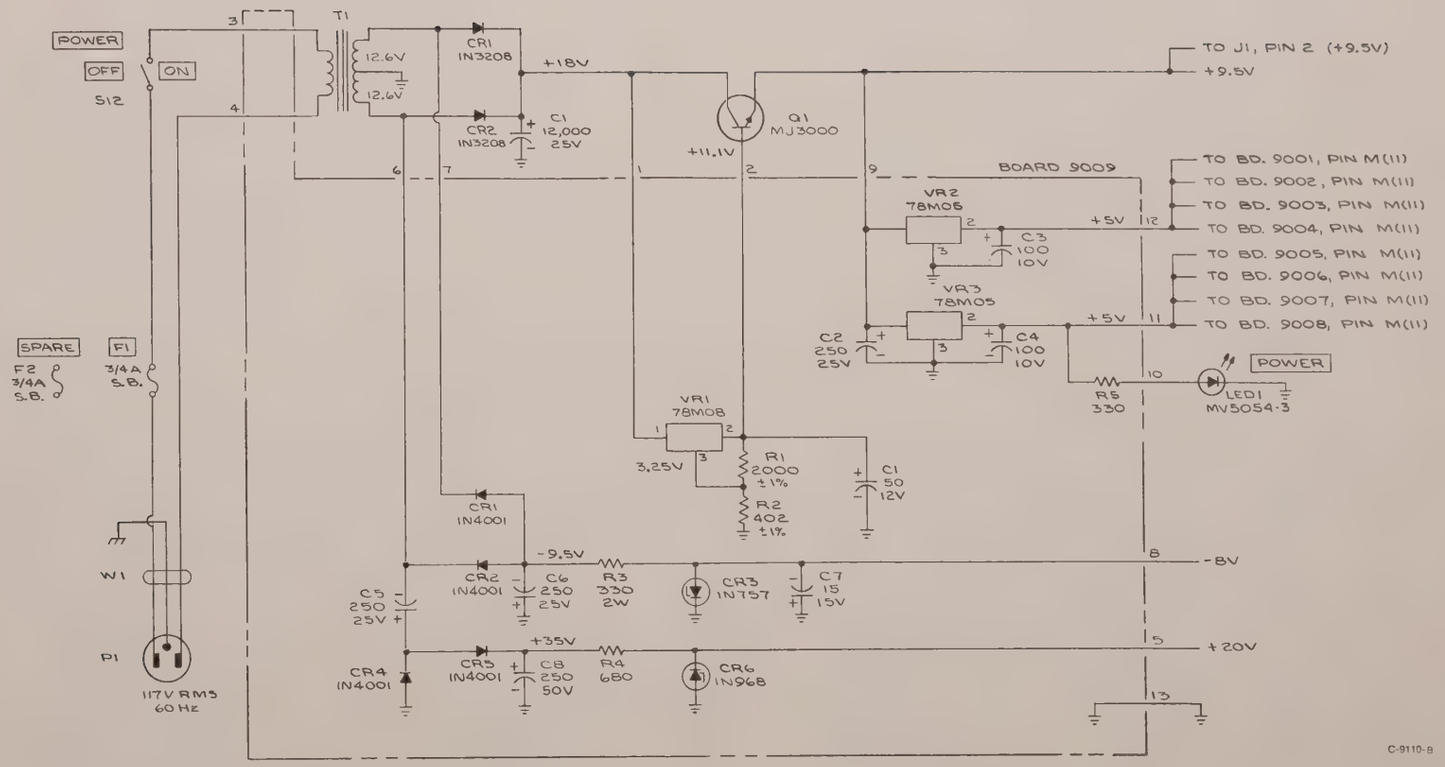
FIGURE 7-13
INTERFACE II
MODEL 2474

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9009 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No. 9028
C1	Capacitor, 50mF, 12V, Sprague No.TE-1133
C2	Capacitor, 250 mF, 25V, Richey
C3,C4	Capacitor, 100 mF, ±20%, 10V, Sprague Type 196D
C5,C6	Capacitor, 250 mF, 25V, Richey
C7	Capacitor, 15 mF, ±10%, 15V, Sprague Type 196D
C8	Capacitor, 250 mF, 50V, Sprague Type TVA 1312
CR1,CR2	Diode, 1N4001
CR3	Diode, 1N757
CR4,CR5	Diode, 1N4001
CR6	Diode, 1N968
R1	Resistor, 2K Ohms, ±1%, 1/8W, IRC No.CEA-TO
R2	Resistor, 402 Ohms, ±1%, 1/8W, IRC No.CEA-TO
R3	Resistor, 330 Ohms, ±10%, 2W, A-B Type HB
R4	Resistor, 680 Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
VR1	Voltage Regulator, Fairchild No.78M08
VR2,VR3	Voltage Regulator, Fairchild No.78M05







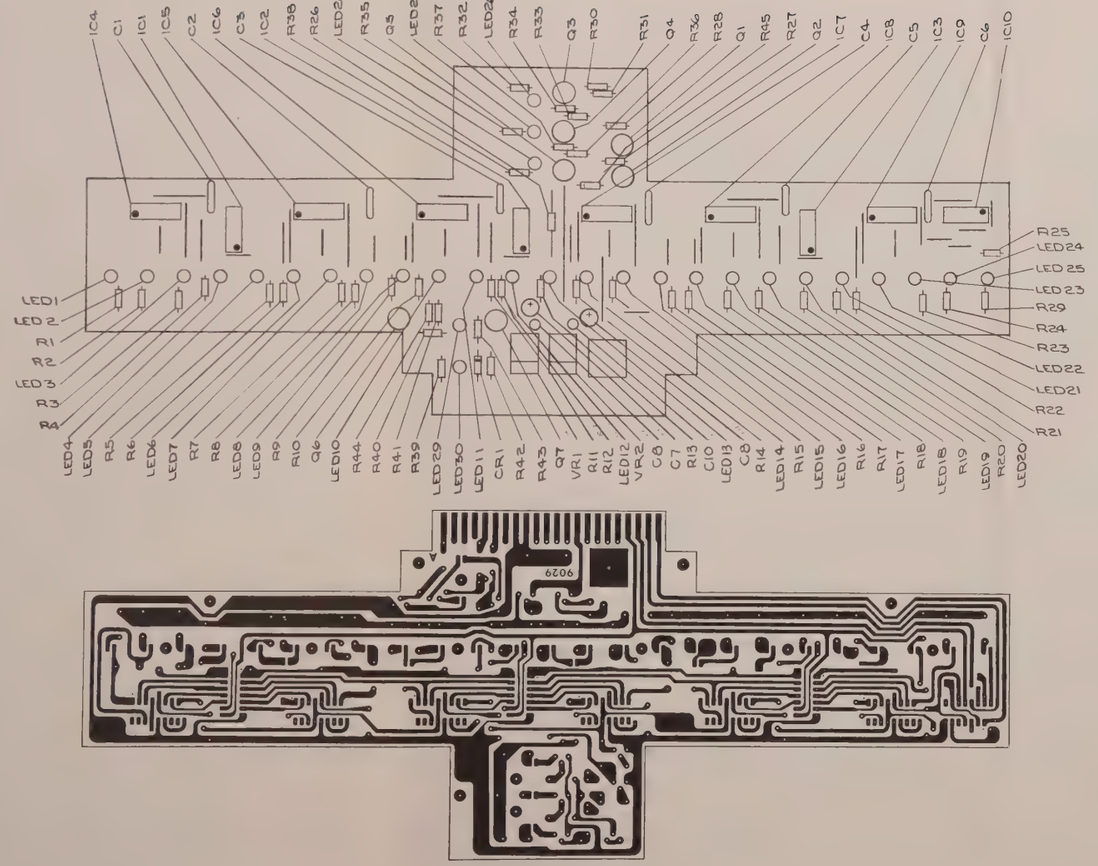
C-9110-8

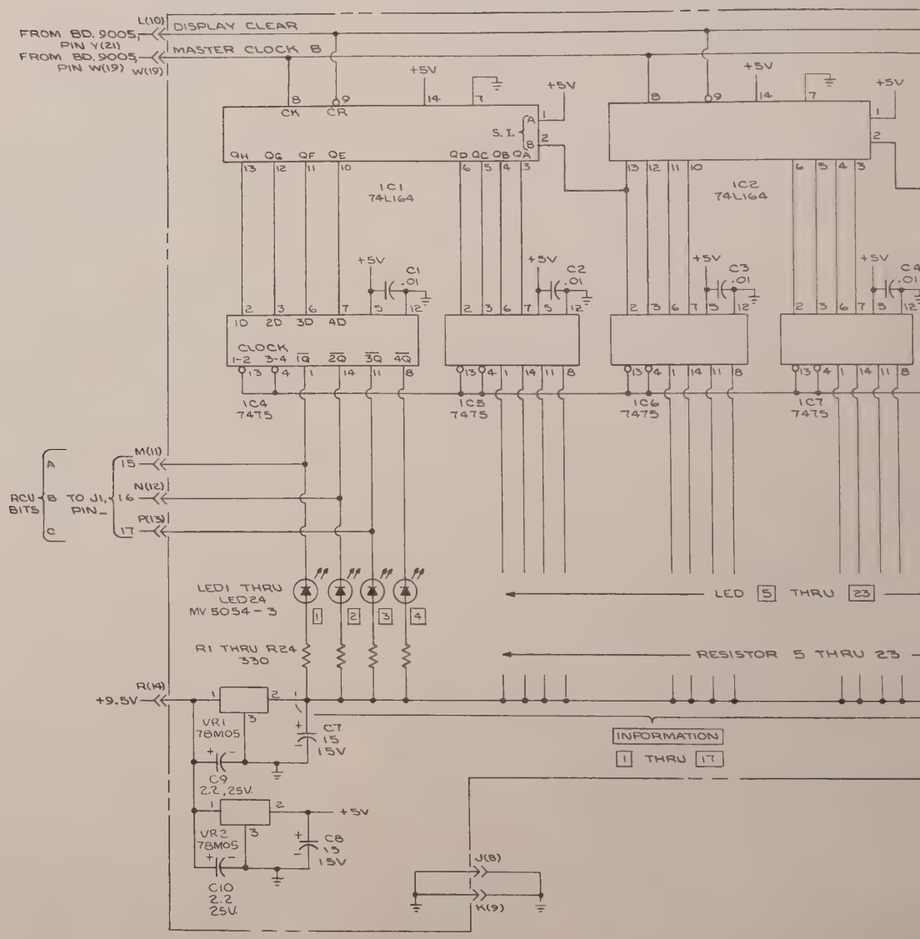
FIGURE 7-14
POWER SUPPLY
MODEL 2474

REPLACEABLE PARTS LIST

QUAN-TECH ASSY. 9010 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9029-2
C1-C6	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C7,C8	Capacitor, 15 mF, ±10%, 15V, Sprague Type 196D
C9, 10	Capacitor, 2.2 mF, ±20%, 25V, Sprague Type 196D
CR1	Diode, 1N276
IC1-IC3	Integrated Circuit, 74L164N
IC4-IC9	Integrated Circuit, 7475N
IC10	Integrated Circuit, 7474N
LED1-LED30	Lamp, Monsanto No.MV-5054-3
Q1-Q7	Transistor, 2N3643
R1-R24	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R25	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R26,R27	Resistor, 470 Ohms, ±10%, 1/4W, A-B Type CB
R28	Resistor, 4700 Ohms, ±10%, 1/4W, A-B Type CB
R29	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R30,R31	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R32	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R33,R34	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R35	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R36,R37	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R38	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R39,R40	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R41	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R42,R43	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R44	Resistor, 330 Ohms, ±10%, 1/4W, A-B Type CB
R45	Resistor, 470 Ohms, ±10%, 1/4W, A-B Type CB
VR1,VR2	Voltage Regulator, Fairchild No.78M05





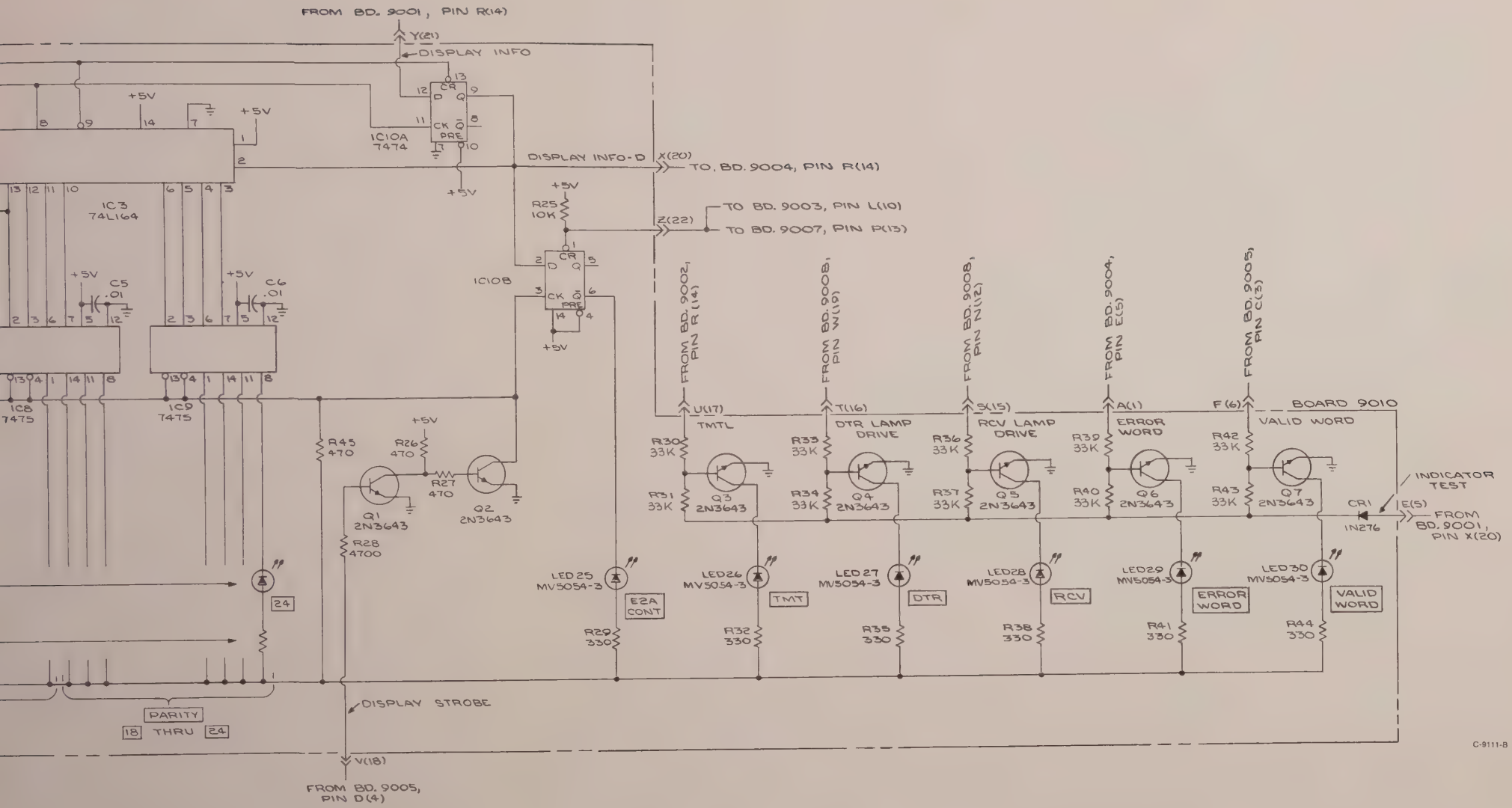
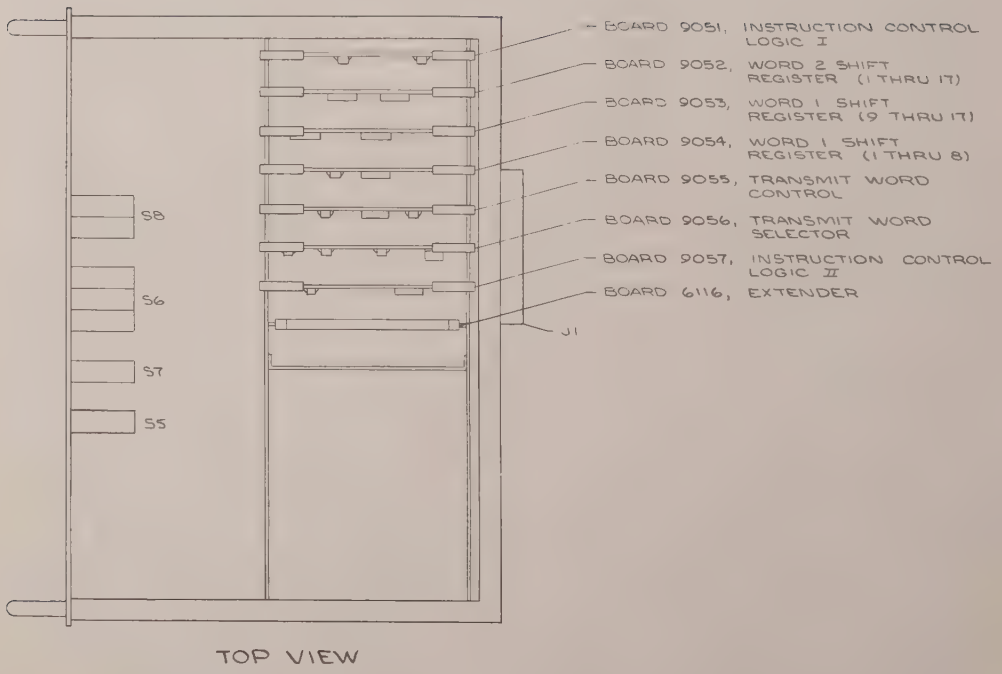


FIGURE 7-15
WORD DISPLAY
MODEL 2474


BOARD 9051, INSTRUCTION CONTROL LOGIC I
BOARD 9052, WORD 2 SHIFT REGISTER (1 THRU 17)
BOARD 9053, WORD 1 SHIFT REGISTER (9 THRU 17)
BOARD 9054, WORD 1 SHIFT REGISTER (1 THRU 8)
BOARD 9055, TRANSMIT WORD CONTROL
BOARD 9056, TRANSMIT WORD SELECTOR
BOARD 9057, INSTRUCTION CONTROL LOGIC II
BOARD 6116, EXTENDER
J1
S8
S6
S7
S5
TOP VIEW

REPLACEABLE PARTS LIST

SYMBOL	DESCRIPTION
	Connector, Cinch Jones No.250-22-30-170 (8 Req'd)
J1	Connector, Amphenol No.26-4401-32P
CR1,CR2	Diode, 1N914B
LED1-LED6	Lamp, Monsanto No.MV-5054-3
S1-S4	Switch, Push Button, Grayhill No.46-01-08-500-0101
S5-S8	Switch, Thumbwheel (One Assembly includes S5, S6, S7 and S8), Quan-Tech No.8566
S9-S11	Switch, Toggle, SPDT, C&K No.7101-SYCB
S12,S13	Switch, Push Button, Grayhill No.46-01-08-500-0101
S14	Switch, Toggle, SPDT, C&K No.7101-SYCB

FIGURE 7-16
COMPONENT AND PRINTED CIRCUIT BOARD LOCATIONS
MODEL 2476

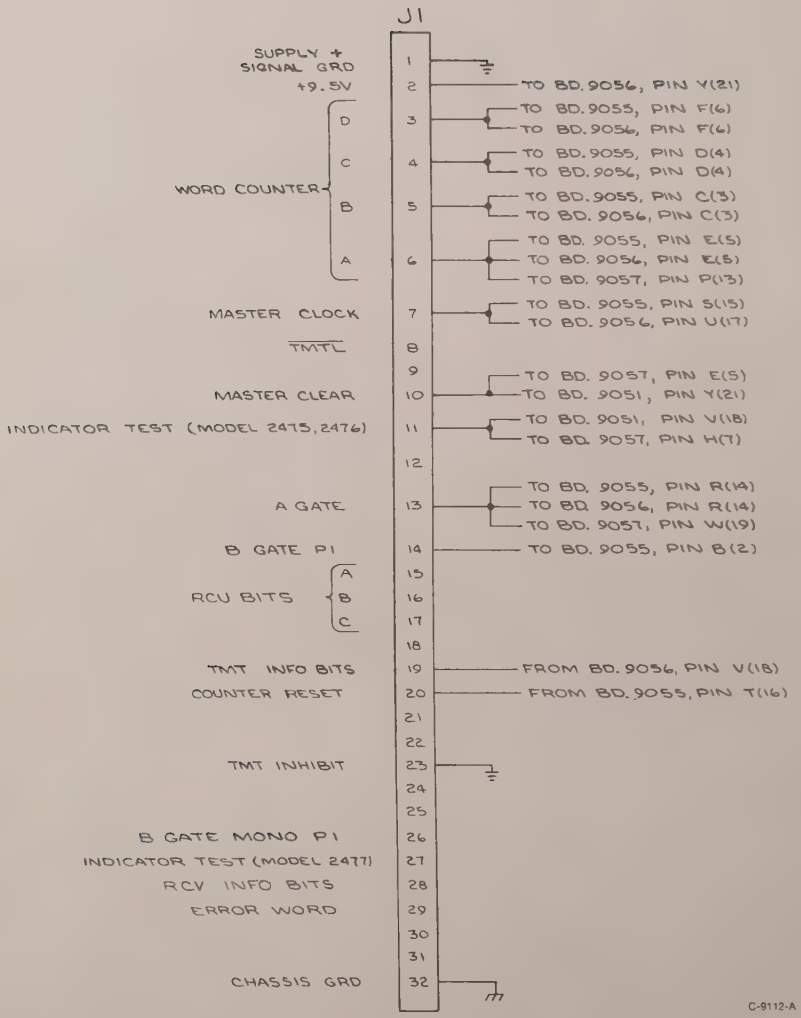
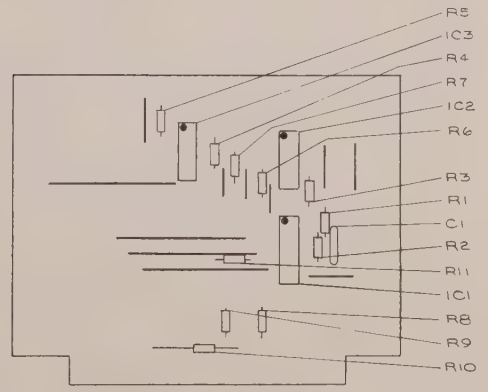
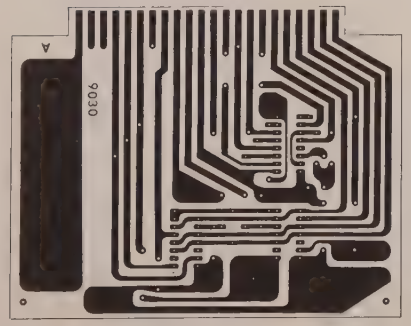


FIGURE 7-17
SCHEMATIC
CONNECTOR (P1 TO BTS)
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9051 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9030 Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
IC1 IC2,IC3	Integrated Circuit, CD4009AE Integrated Circuit, CD4013AE
R1 R2 R3-R6 R7 R8-R11	Resistor, 1 MegOhm, ±10%, 1/4W, A-B Type CB Resistor, 470K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 220 Ohms, ±10%, 1/4W, A-B Type CB





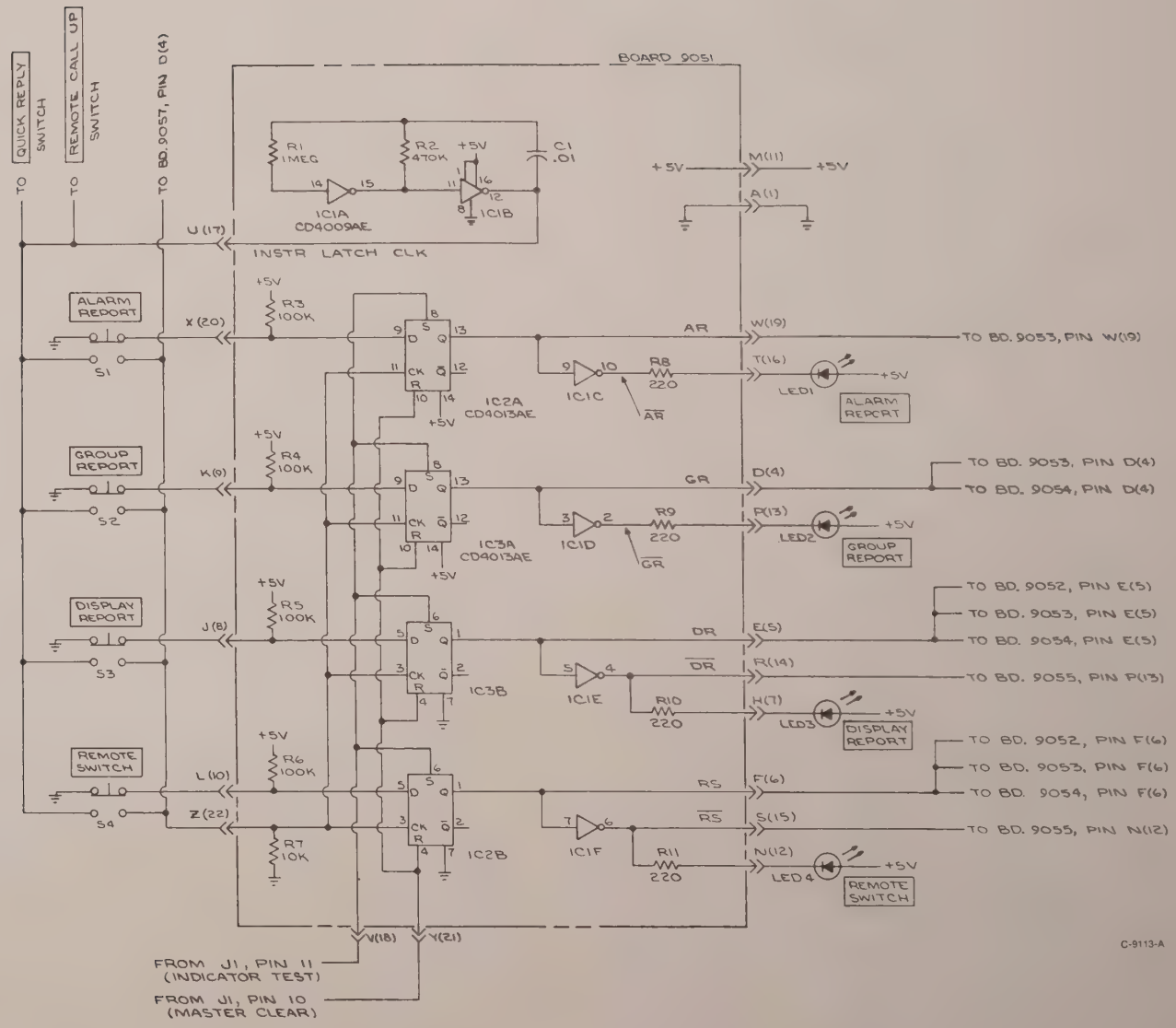
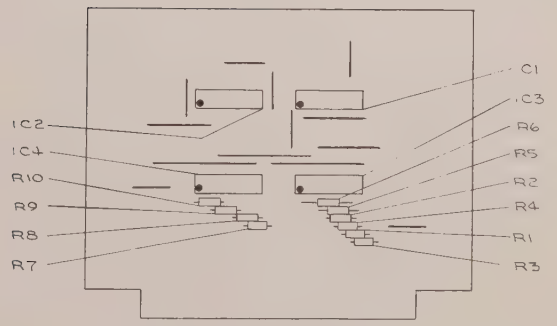
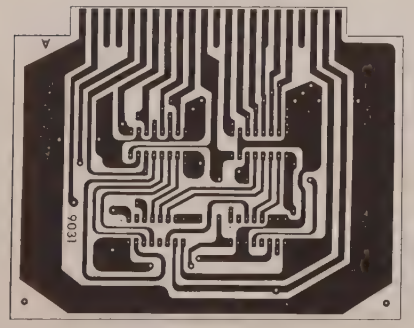


FIGURE 7-18
INSTRUCTION CONTROL LOGIC I
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9052 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9031 Ejector, SAE No.6100 (2 Req'd)
IC1,IC2	Integrated Circuit, CD4021AE
IC3,IC4	Integrated Circuit, CD4019AE
R1-R10	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





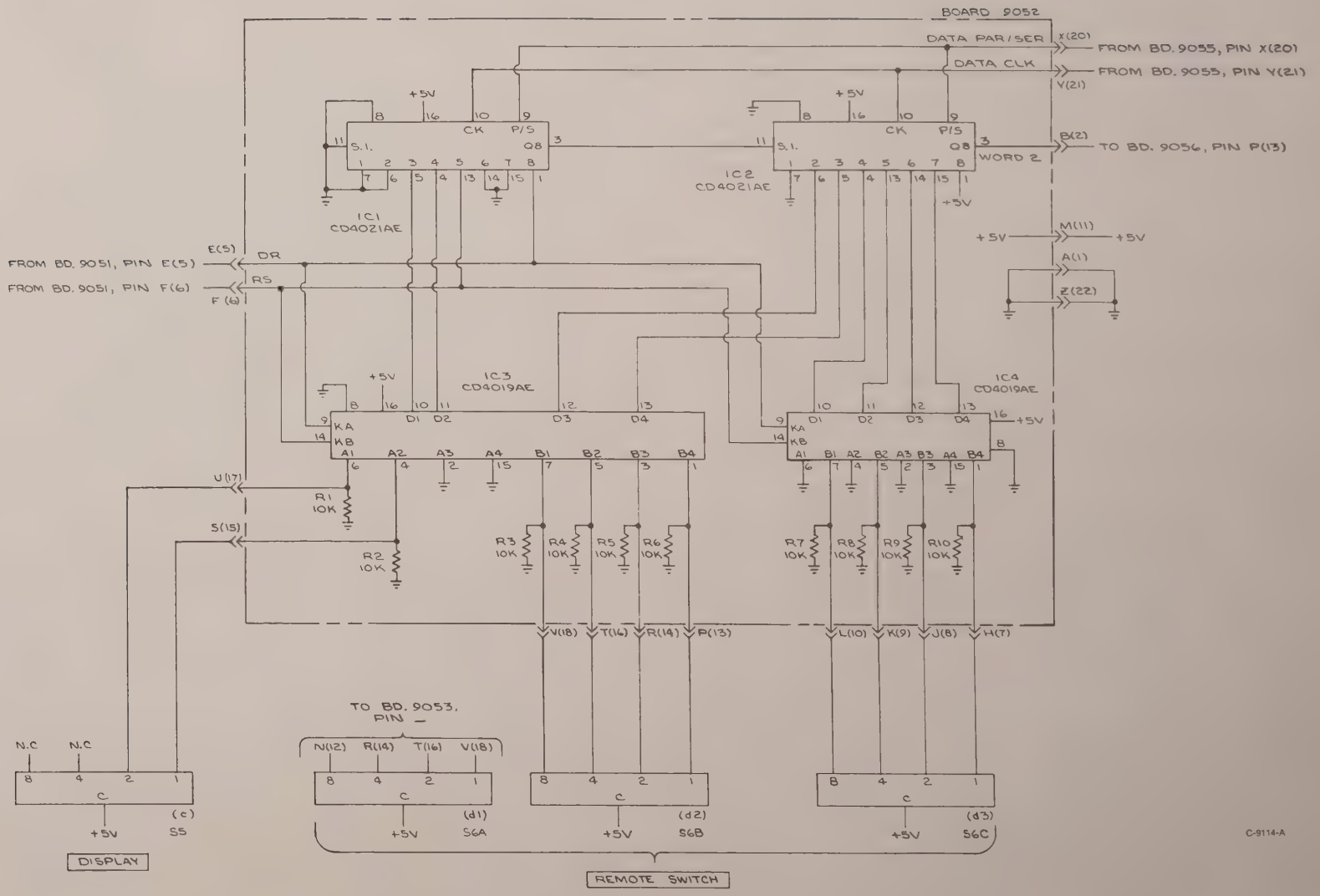
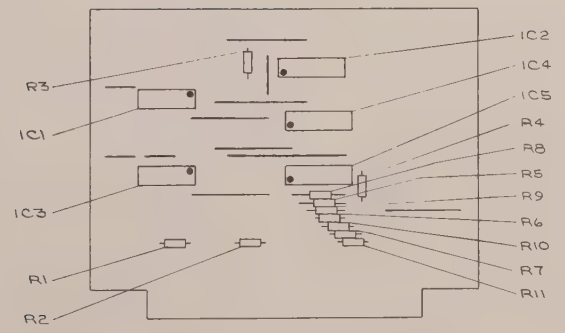
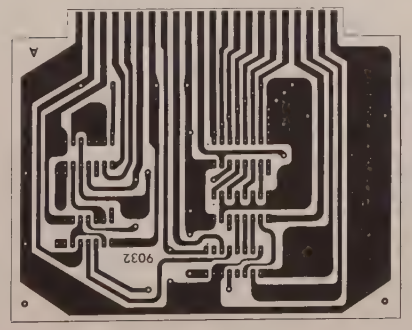


FIGURE 7-19
WORD 2 SHIFT REGISTER (BITS 1 THRU 17)
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9053 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9032 Ejector, SAE No.6100 (2 Req'd)
IC1	Integrated Circuit, CD4001AE
IC2	Integrated Circuit, CD4021AE
IC3	Integrated Circuit, CD4025AE
IC4,IC5	Integrated Circuit, CD4019AE
R1,R2	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R3-R11	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





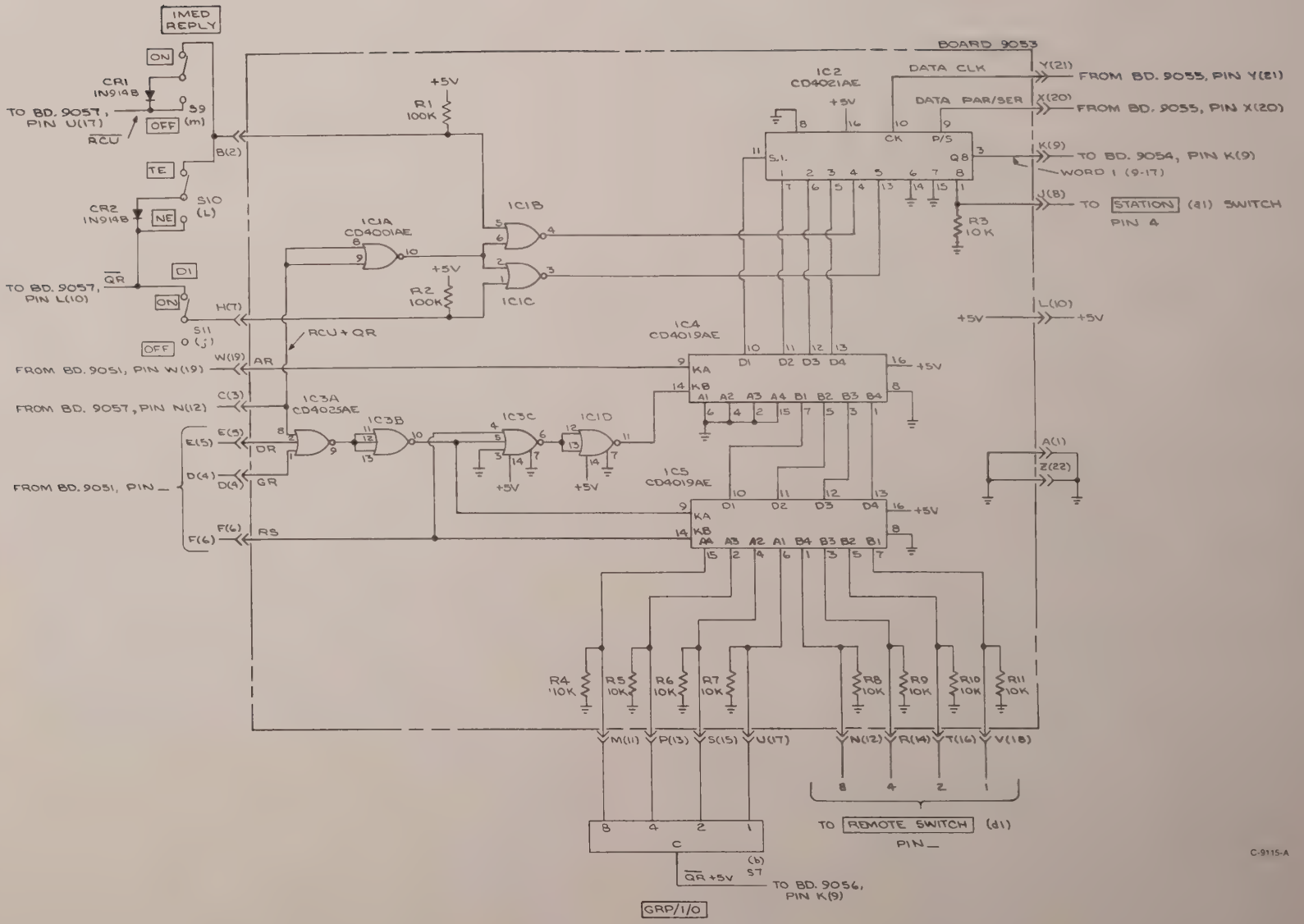
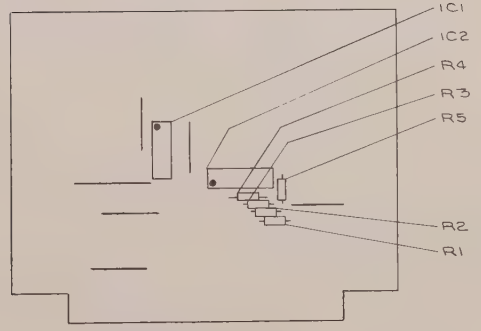
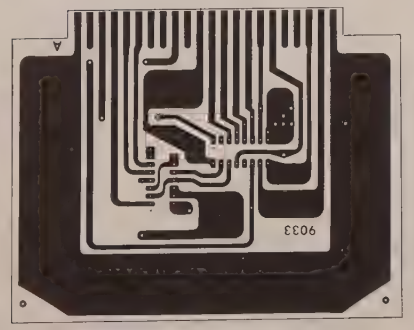


FIGURE 7-20
WORD 1 SHIFT REGISTER (BITS 9 THRU 17)
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9054 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9033 Ejector, SAE No.6100 (2 Req'd)
IC1	Integrated Circuit, CD4001AE
IC2	Integrated Circuit, CD4021AE
R1-R5	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





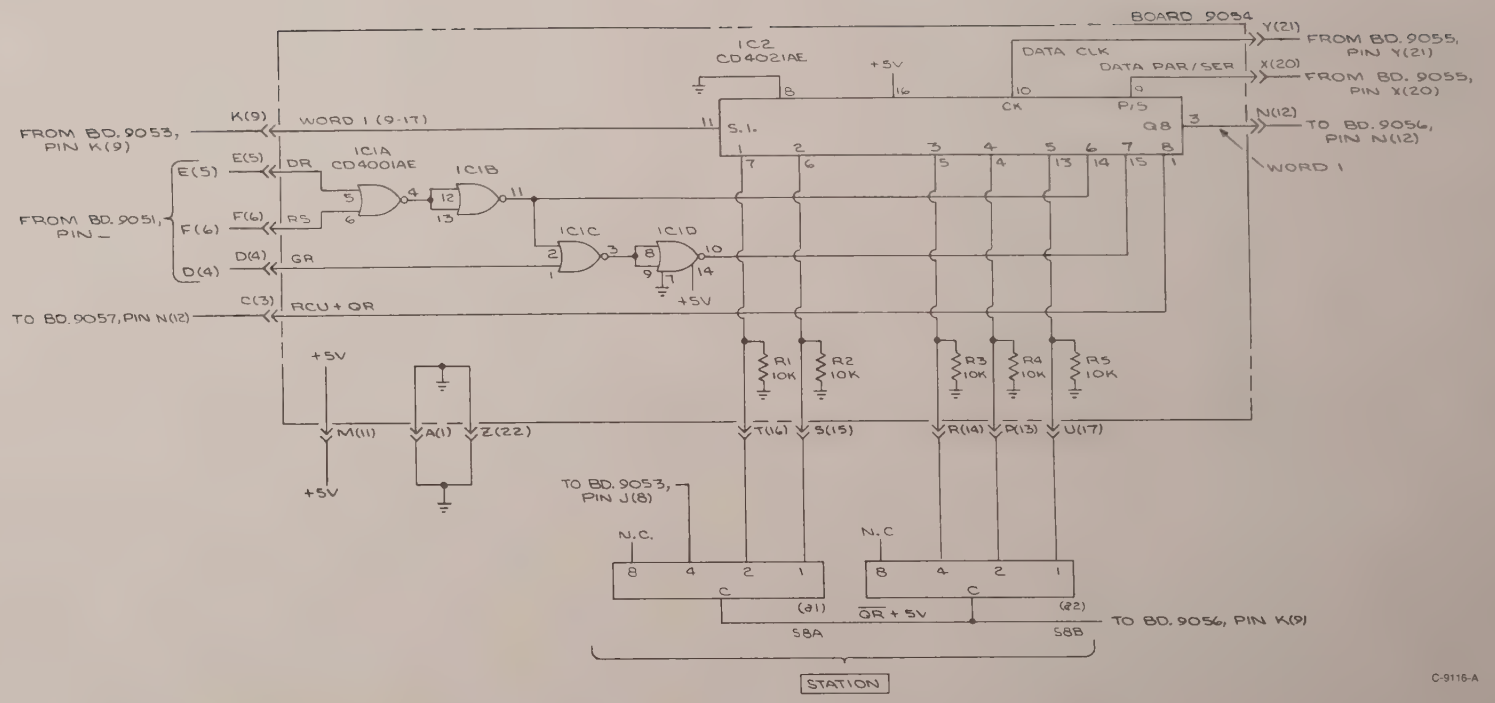
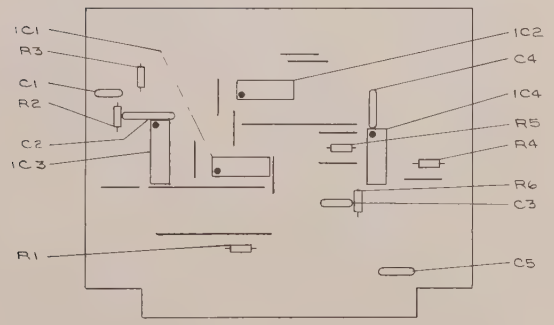
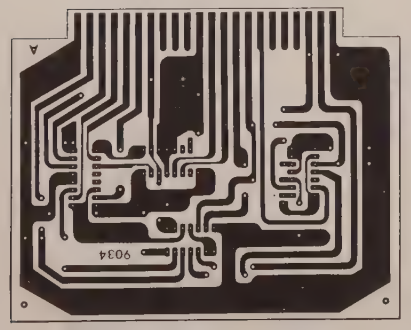


FIGURE 7-21
WORD 1 SHIFT REGISTER (BITS 1 THRU 8)
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9055 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9034
	Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C2	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C3	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C4	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C5	Capacitor, 47 pF, ±10%, 1000V, Centralab No.DD-470
IC1	Integrated Circuit, CD4012AE
IC2	Integrated Circuit, CD4011AE
IC3	Integrated Circuit, 74L85N
IC4	Integrated Circuit, CD4013AE
R1,R2	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 15K Ohms, ±10%, 1/4W, A-B Type CB
R5,R6	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB





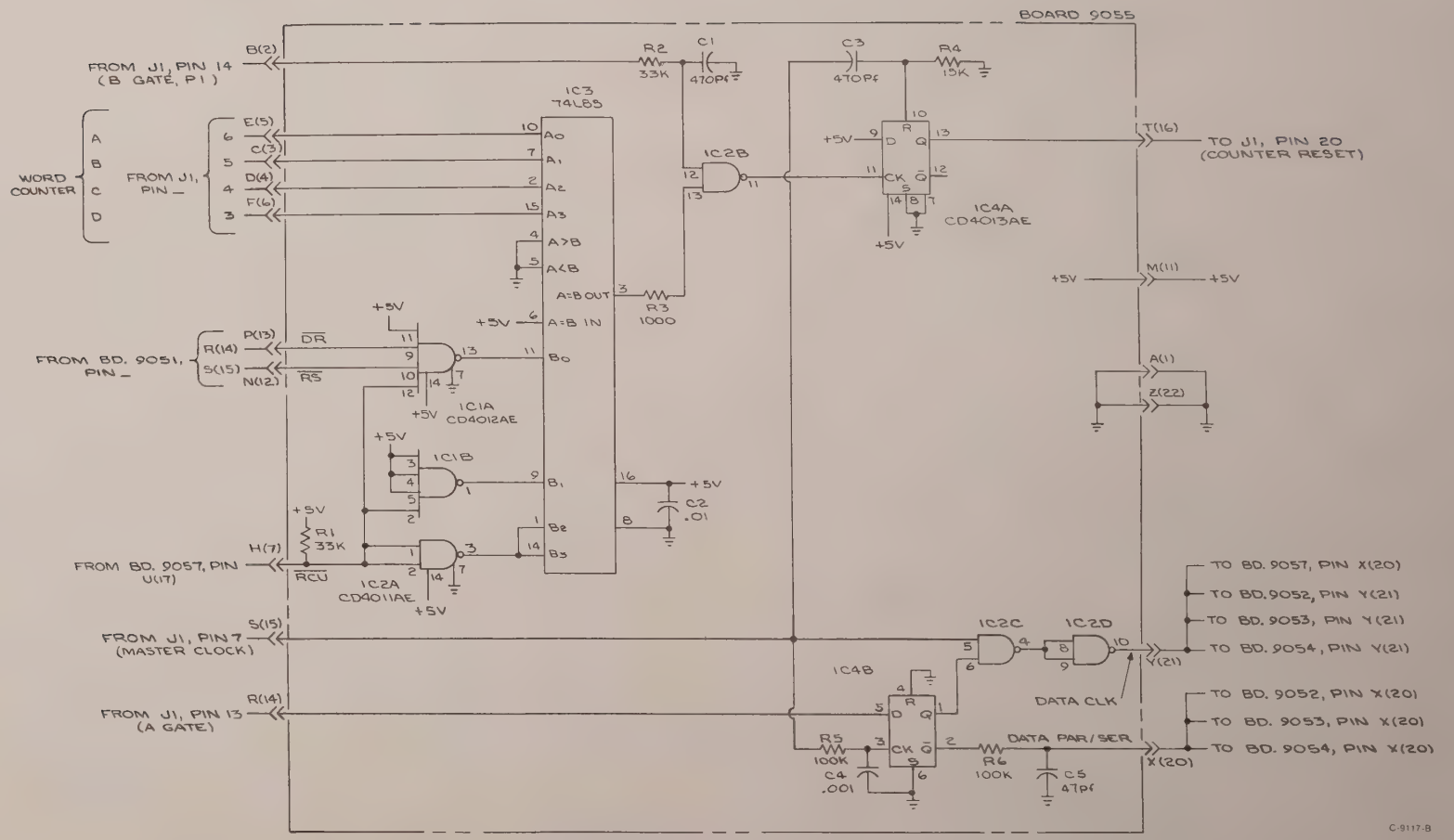
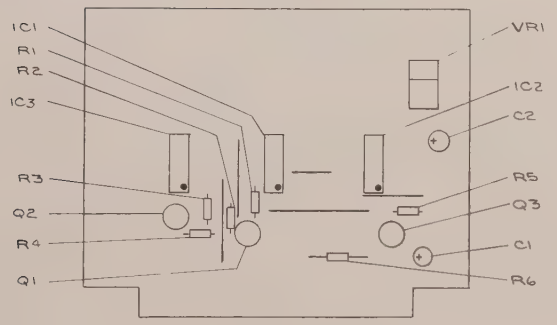
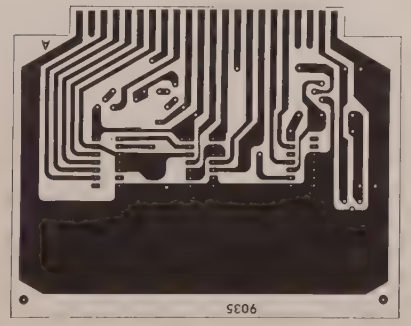


FIGURE 7-22
TRANSMIT WORD CONTROL
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9056 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9035
	Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 15 mF, ±10%, 15V, Sprague Type 196D
C2	Capacitor, 100 mF, ±20%, 10V, Sprague Type 196D
IC1	Integrated Circuit, CD4016AE
IC2	Integrated Circuit, CD4013AE
IC3	Integrated Circuit, CD4002AE
Q1	Transistor, 2N3643
Q2	Transistor, 2N3644
Q3	Transistor, 2N3643
R1,R2	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
VR1	Voltage Regulator, Fairchild No.78M05





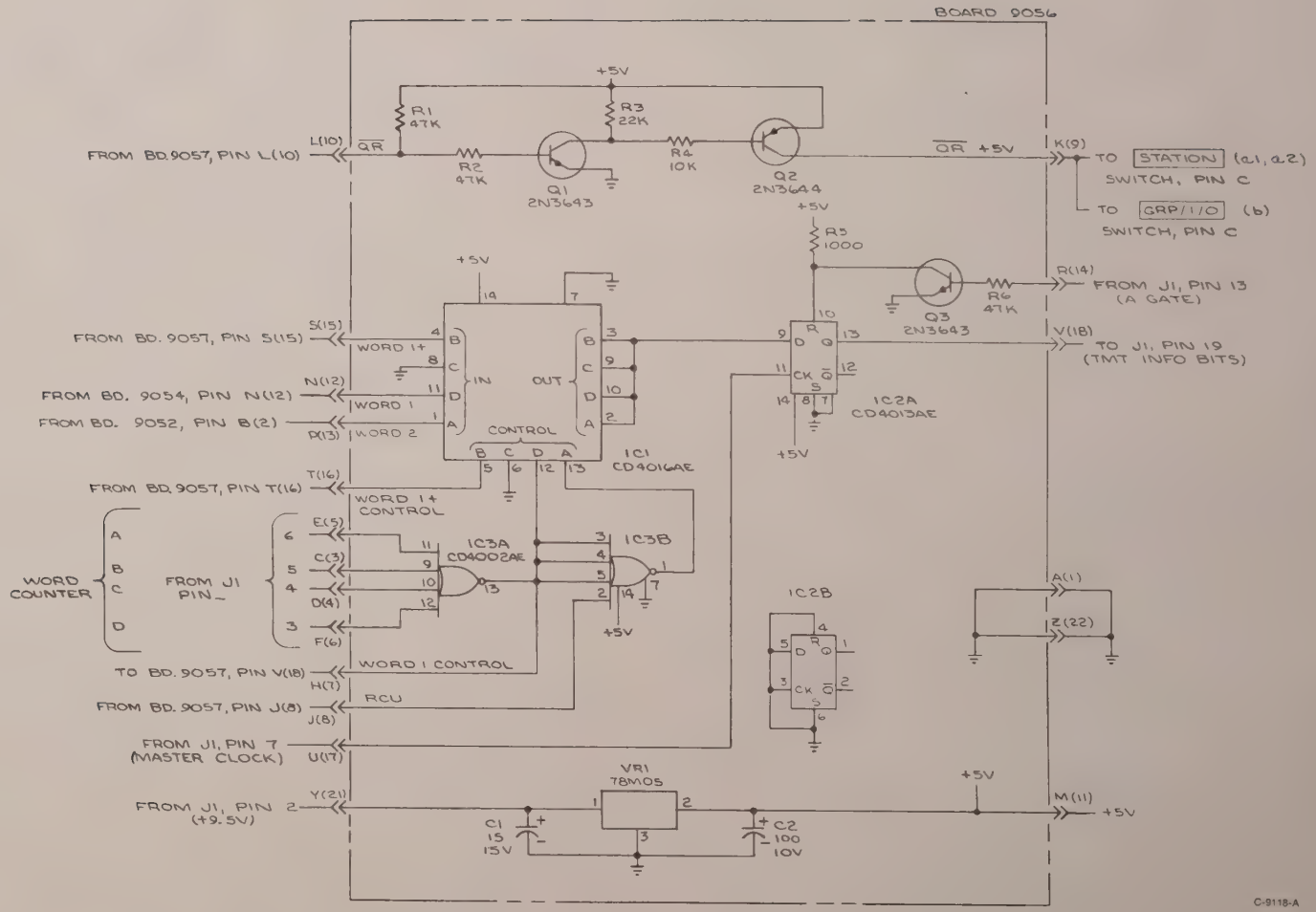
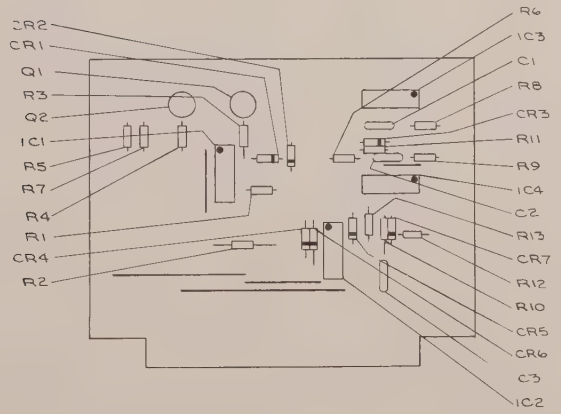
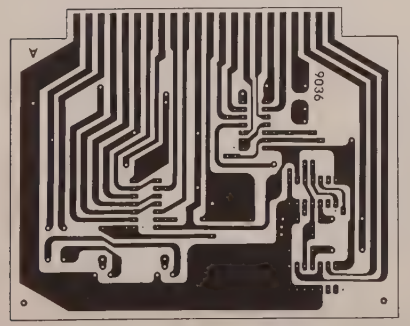


FIGURE 7-23
TRANSMIT WORD SELECTOR
MODEL 2476

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9057 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9036 Ejector, SAE No.6100 (2 Req'd)
C1-C3	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
CR1-CR7	Diode, 1N914B
IC1	Integrated Circuit, CD4013AE
IC2	Integrated Circuit, CD4001AE
IC3,IC4	Integrated Circuit, CD4013AE
Q1,Q2	Transistor, 2N3643
R1,R2	Resistor, 100K Ohms,±10%, 1/4W, A-B Type CB
R3,R4	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 220 Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R7	Resistor, 220 Ohms, ±10%, 1/4W, A-B Type CB
R8	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 68K Ohms, ±10%, 1/4W, A-B Type CB
R10	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R11	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R12	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R13	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB





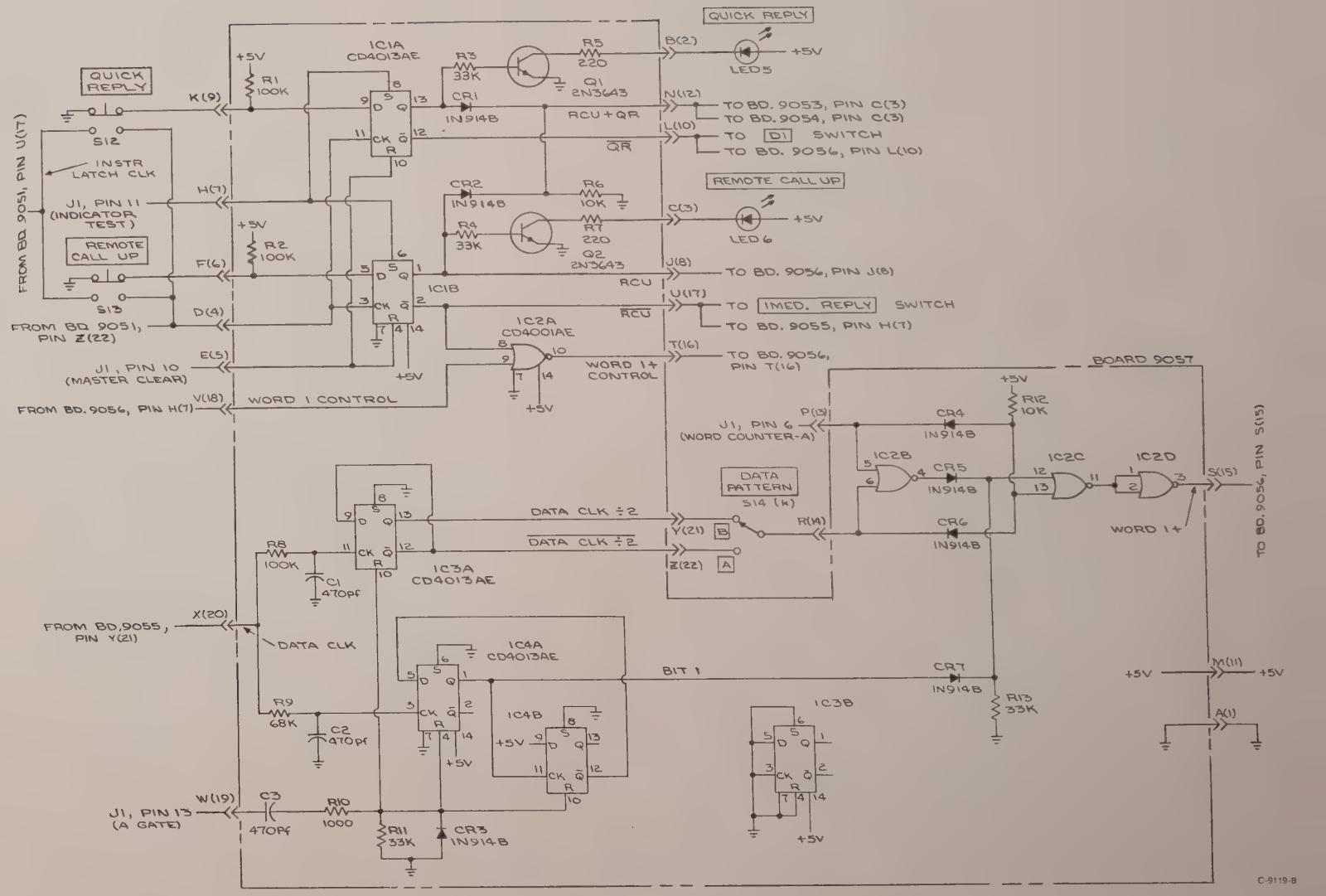
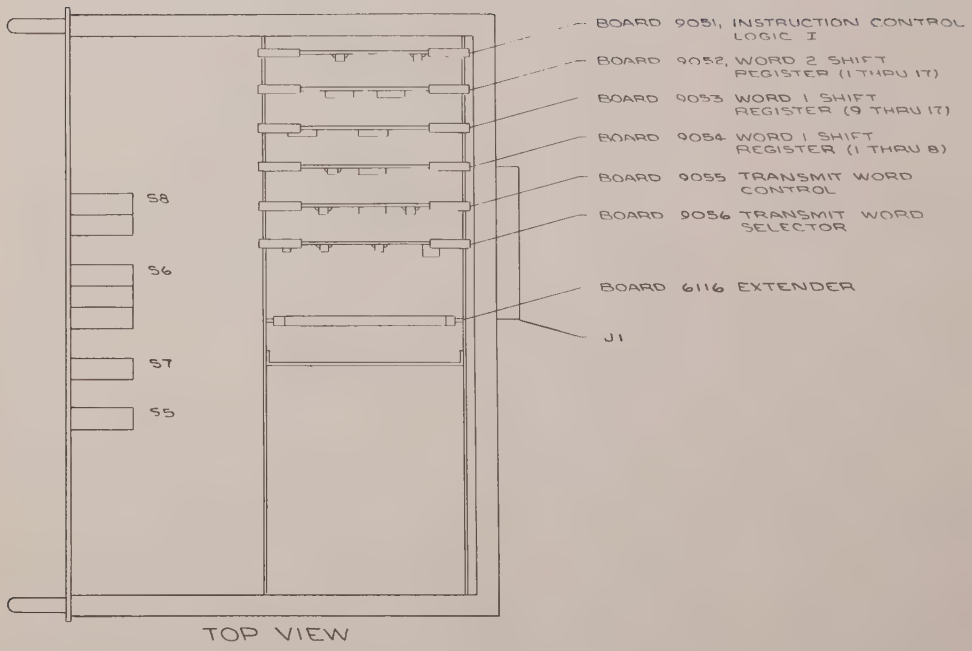


FIGURE 7-24
INSTRUCTION CONTROL LOGIC II
MODEL 2476


BOARD 9051, INSTRUCTION CONTROL LOGIC I
BOARD 9052, WORD 2 SHIFT REGISTER (1 THRU 17)
BOARD 9053 WORD 1 SHIFT REGISTER (9 THRU 17)
BOARD 9054 WORD 1 SHIFT REGISTER (1 THRU 8)
BOARD 9055 TRANSMIT WORD CONTROL
BOARD 9056 TRANSMIT WORD SELECTOR
BOARD 6116 EXTENDER
J1
S8
S6
S7
S5
TOP VIEW

REPLACEABLE PARTS LIST

SYMBOL	DESCRIPTION
	Connector, Cinch Jones No.250-22-30-170 (7 Req'd)
J1	Connector, Amphenol No.26-4401-32P
LED1-LED4	Lamp, Monsanto, No.MV-5054-3
S1-S4	Switch, Push Button, Grayhill No.46-01-08-500-0101
S5-S8	Switch, Thumbwheel (One Assembly includes S5, S6, S7 and S8) Quan-Tech No.8566

FIGURE 7-25
COMPONENT AND PRINTED CIRCUIT BOARD LOCATIONS
MODEL 2475

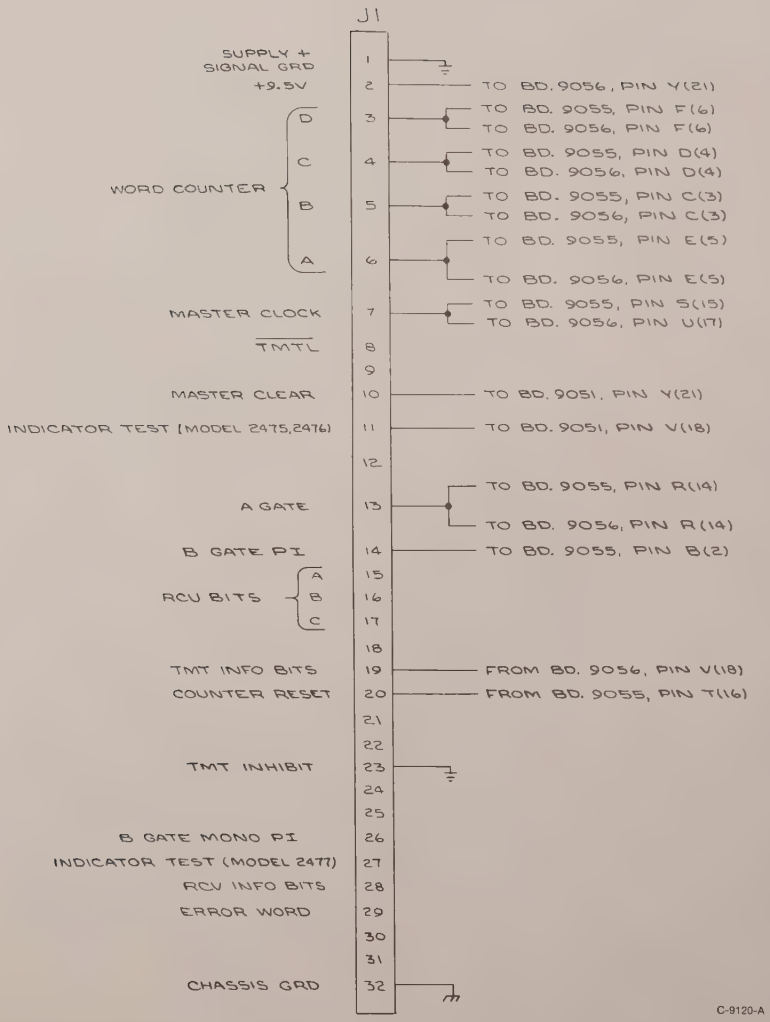
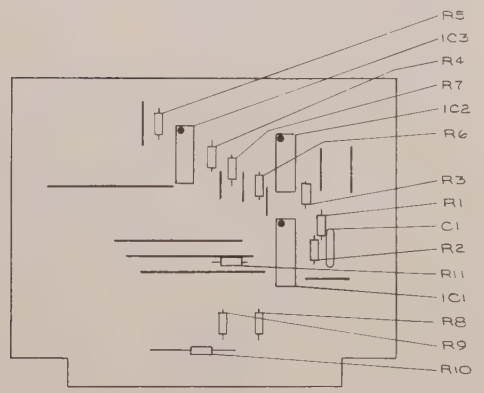
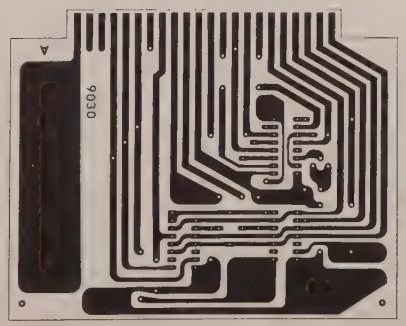


FIGURE 7-26
SCHEMATIC
CONNECTOR (PI TO BTS)
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9051 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9030 Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
IC1 IC2,IC3	Integrated Circuit, CD4009AE Integrated Circuit, CD4013AE
R1 R2 R3-R6 R7 R8-R11	Resistor, 1 MegOhm, ±10%, 1/4W, A-B Type CB Resistor, 470K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB Resistor, 220 Ohms, ±10%, 1/4W, A-B Type CB





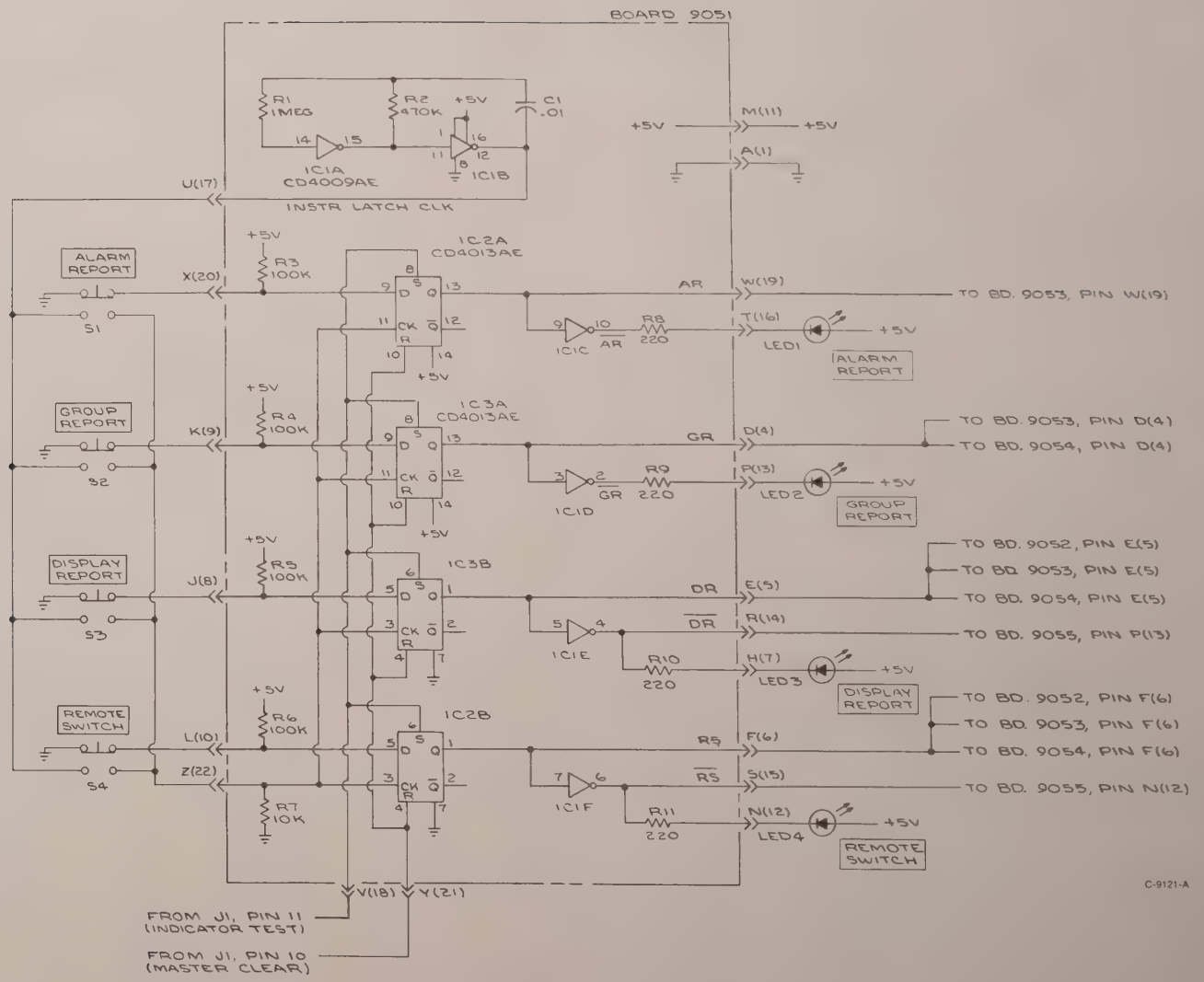
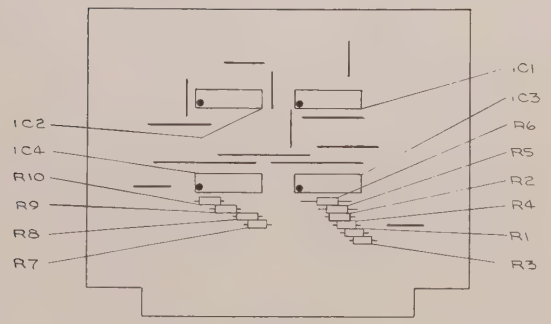
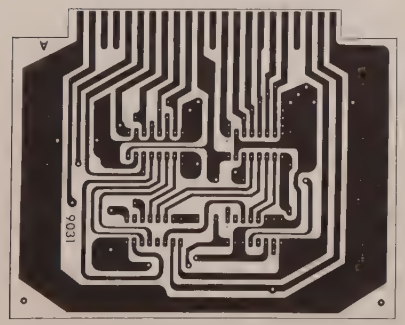


FIGURE 7-27
INSTRUCTION CONTROL LOGIC I
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9052 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9031 Ejector, SAE No.6100 (2 Req'd)
IC1,IC2 IC3,IC4	Integrated Circuit, CD4021AE Integrated Circuit, CD4019AE
R1-R10	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





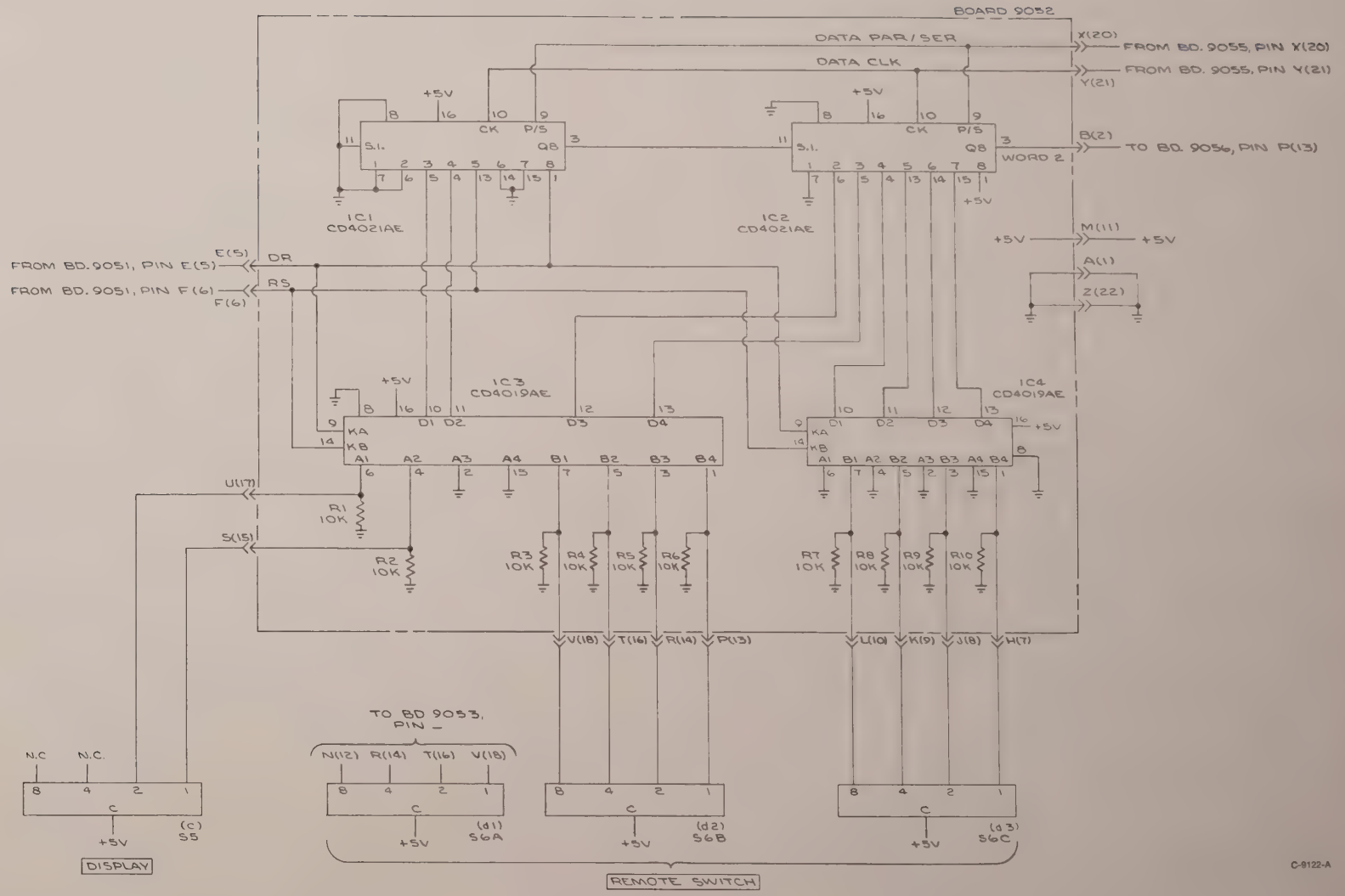
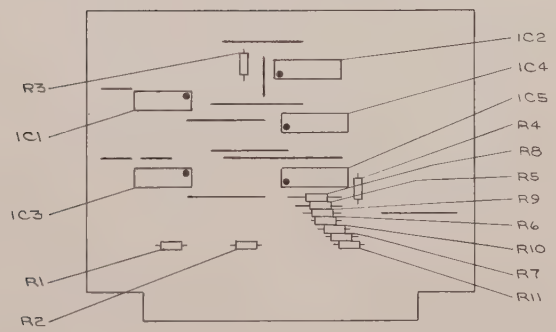
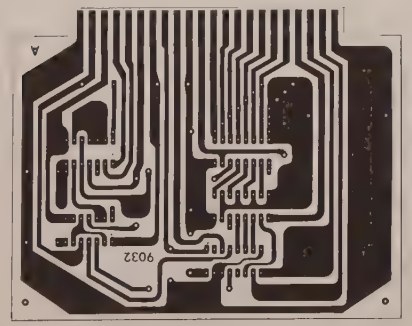


FIGURE 7-28
WORD 2 SHIFT REGISTER (BITS 1 THRU 17)
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9053 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9032 Ejector, SAE No.6100 (2 Req'd)
IC1	Integrated Circuit, CD4001AE
IC2	Integrated Circuit, CD4021AE
IC3	Integrated Circuit, CD4025AE
IC4,IC5	Integrated Circuit, CD4019AE
R1,R2	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R3-R11	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





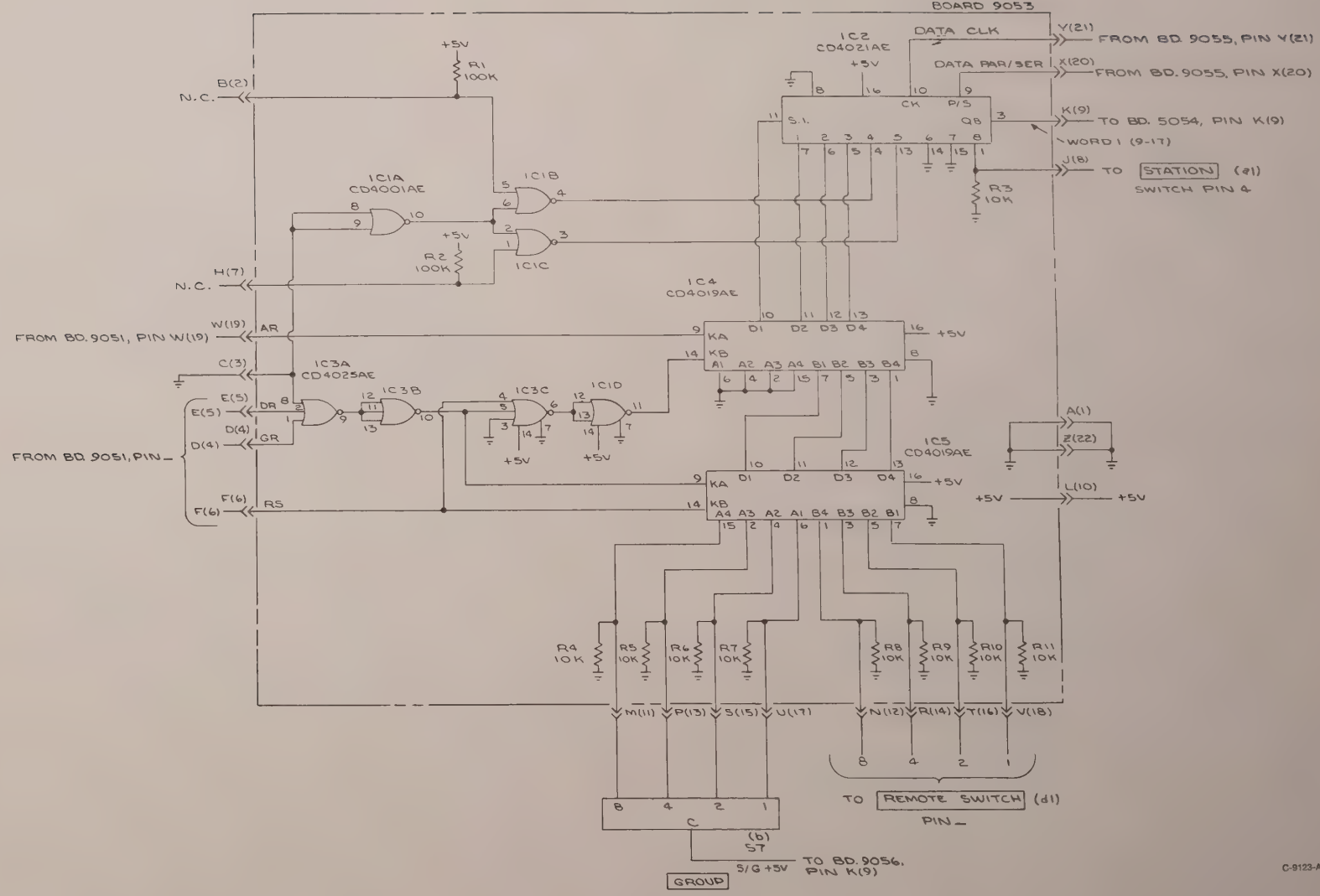
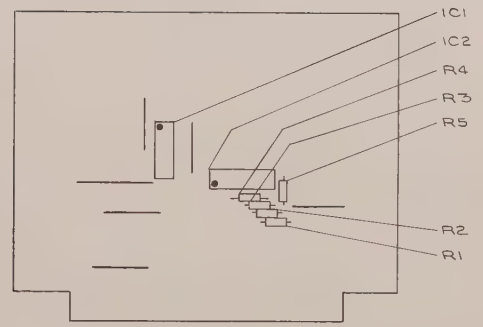
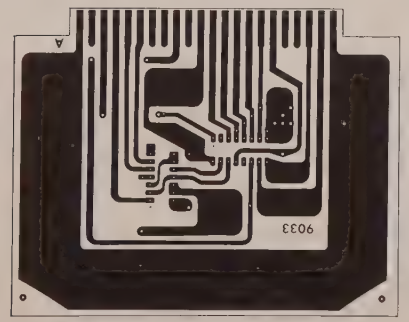


FIGURE 7-29
WORD 1 SHIFT REGISTER (BITS 9 THRU 17)
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9054 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9033 Ejector, SAE No.6100 (2 Req'd)
IC1 IC2	Integrated Circuit, CD4001AE Integrated Circuit, CD4021AE
R1-R5	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB





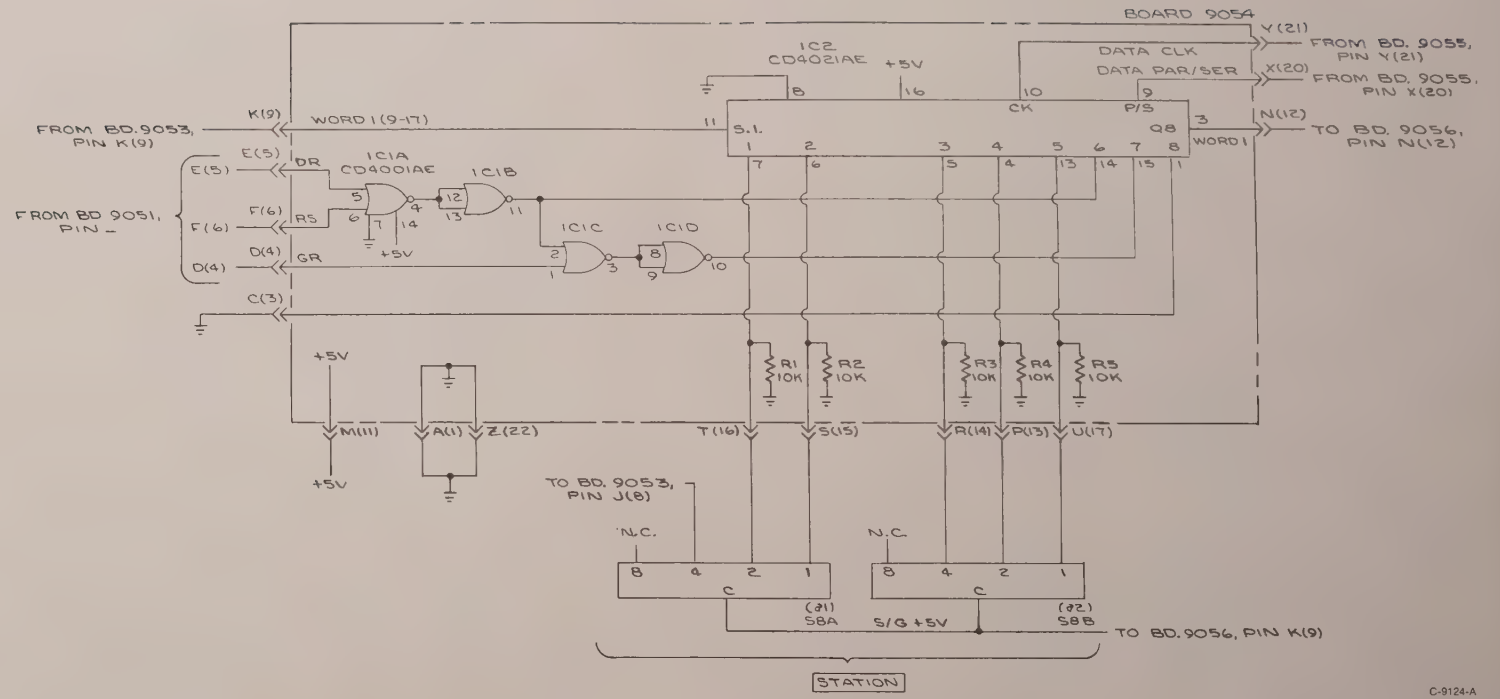
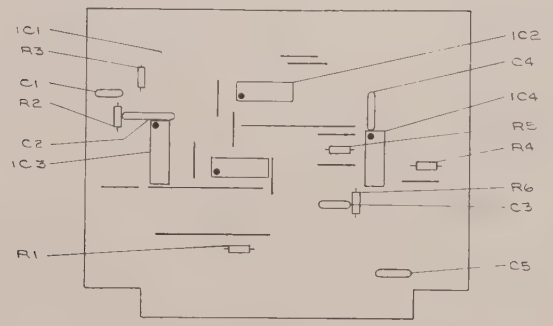
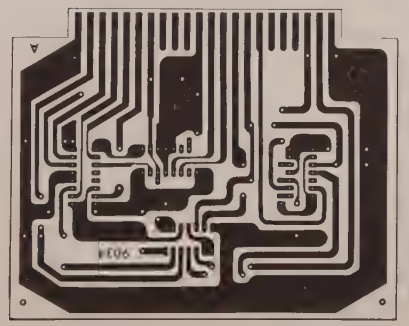


FIGURE 7-30
WORD 1 SHIFT REGISTER (BITS 1 THRU 8)
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9055 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9034
	Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C2	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C3	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C4	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C5	Capacitor, 47 pF, ±10%, 1000V, Centralab No.DD-470
IC1	Integrated Circuit, CD4012AE
IC2	Integrated Circuit, CD4011AE
IC3	Integrated Circuit, 74L85N
IC4	Integrated Circuit, CD4013AE
R1,R2	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 15K Ohms, ±10%, 1/4W, A-B Type CB
R5,R6	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB





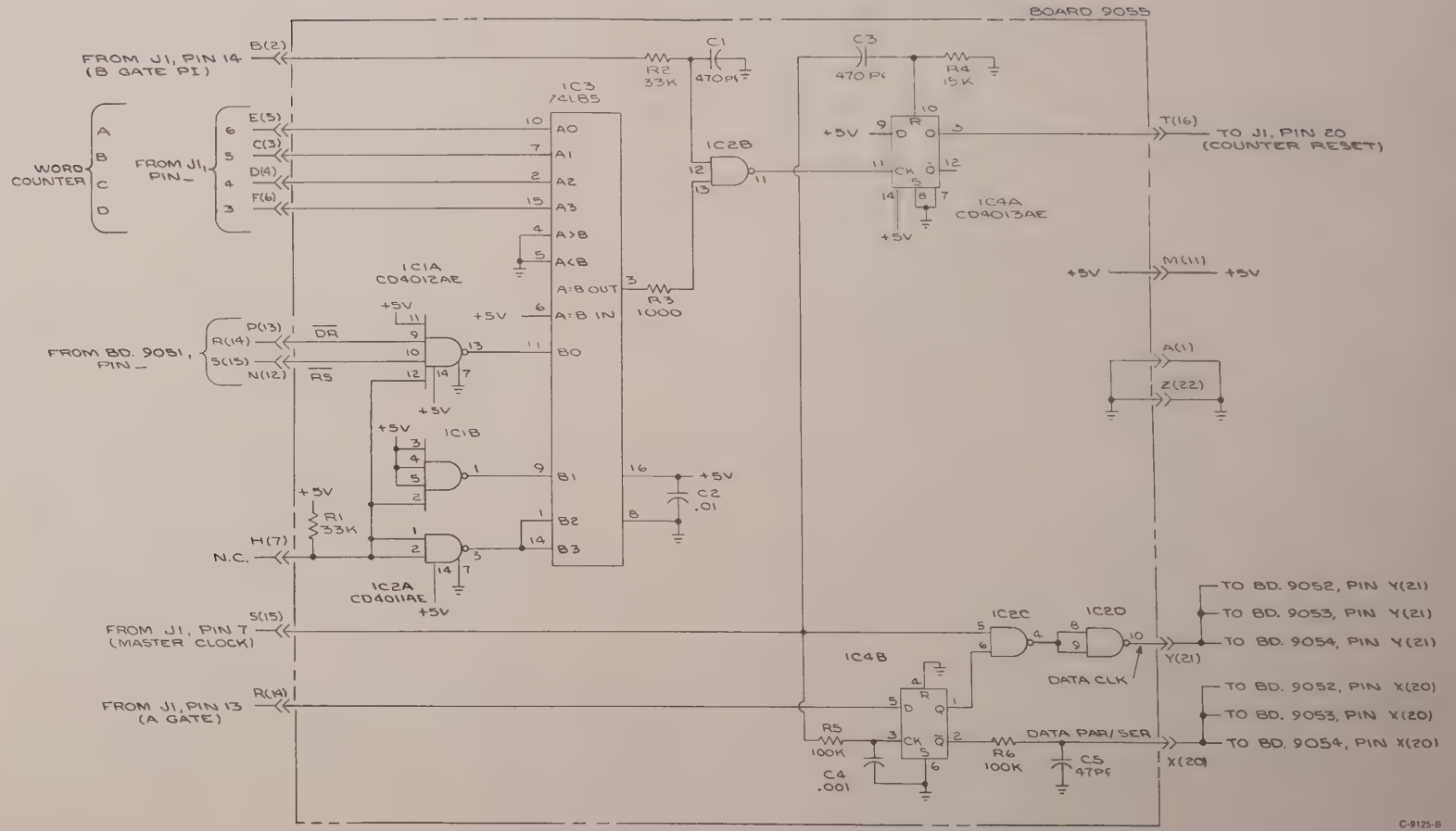
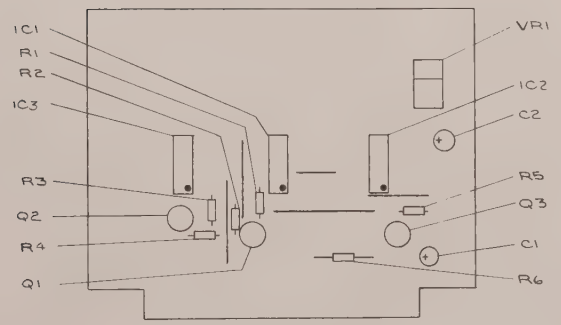
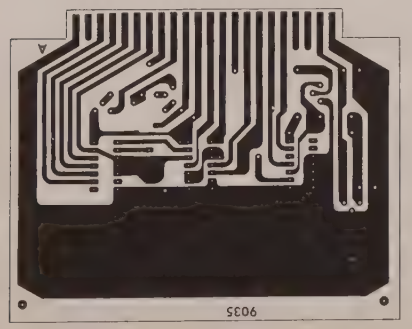


FIGURE 7-31
TRANSMIT WORD CONTROL
MODEL 2475

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9056 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9035 Ejector, SAE No.6100 (2 Req'd)
C1	Capacitor, 15 mF, ±10%, 15V, Sprague Type 196D
C2	Capacitor, 100 mF, ±20%, 10V, Sprague Type 196D
IC1	Integrated Circuit, CD4016AE
IC2	Integrated Circuit, CD4013AE
IC3	Integrated Circuit, CD4002AE
Q1	Transistor, 2N3643
Q2	Transistor, 2N3644
Q3	Transistor, 2N3643
R1,R2	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R4	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
VR1	Voltage Regulator, Fairchild No.78M05





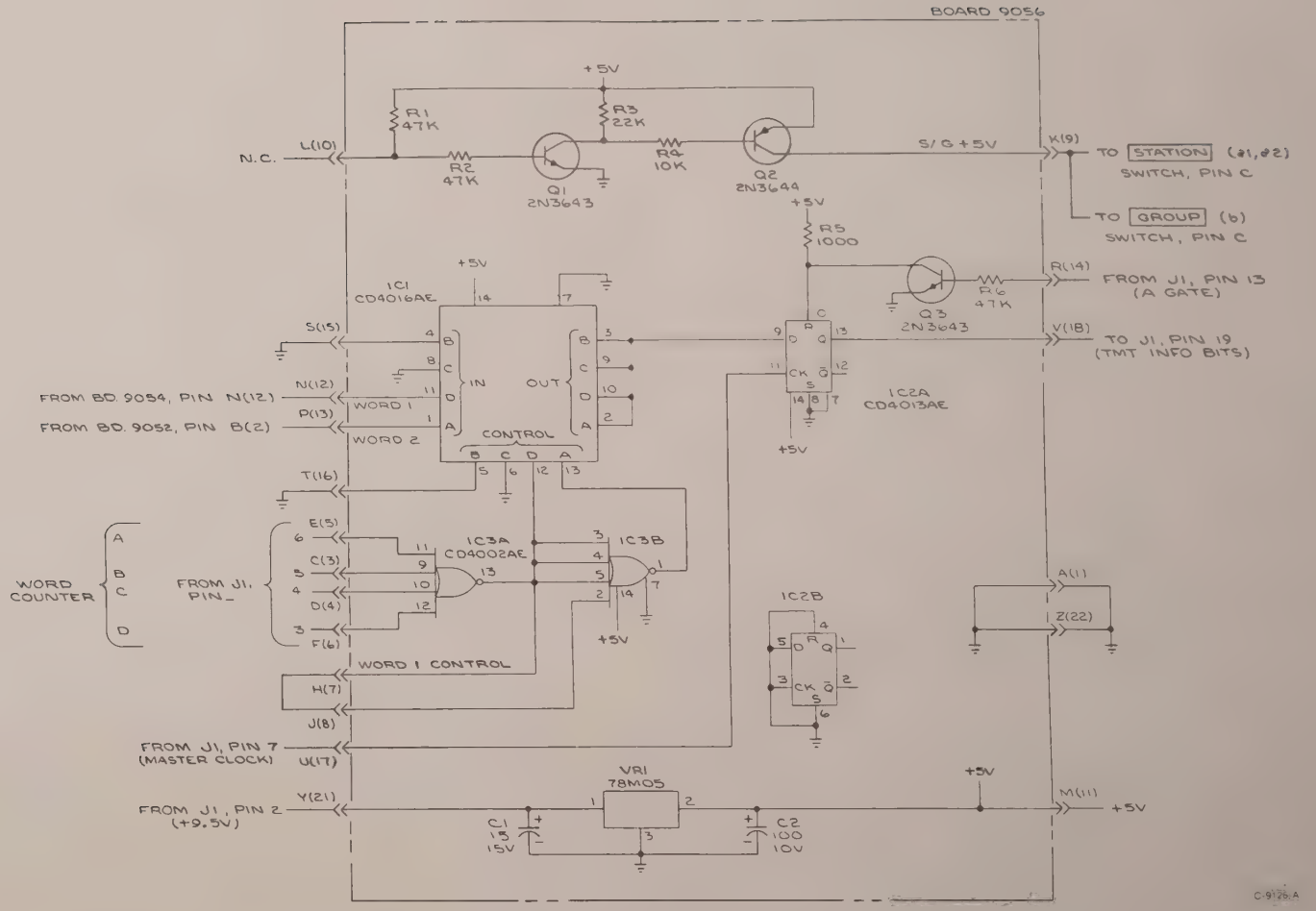
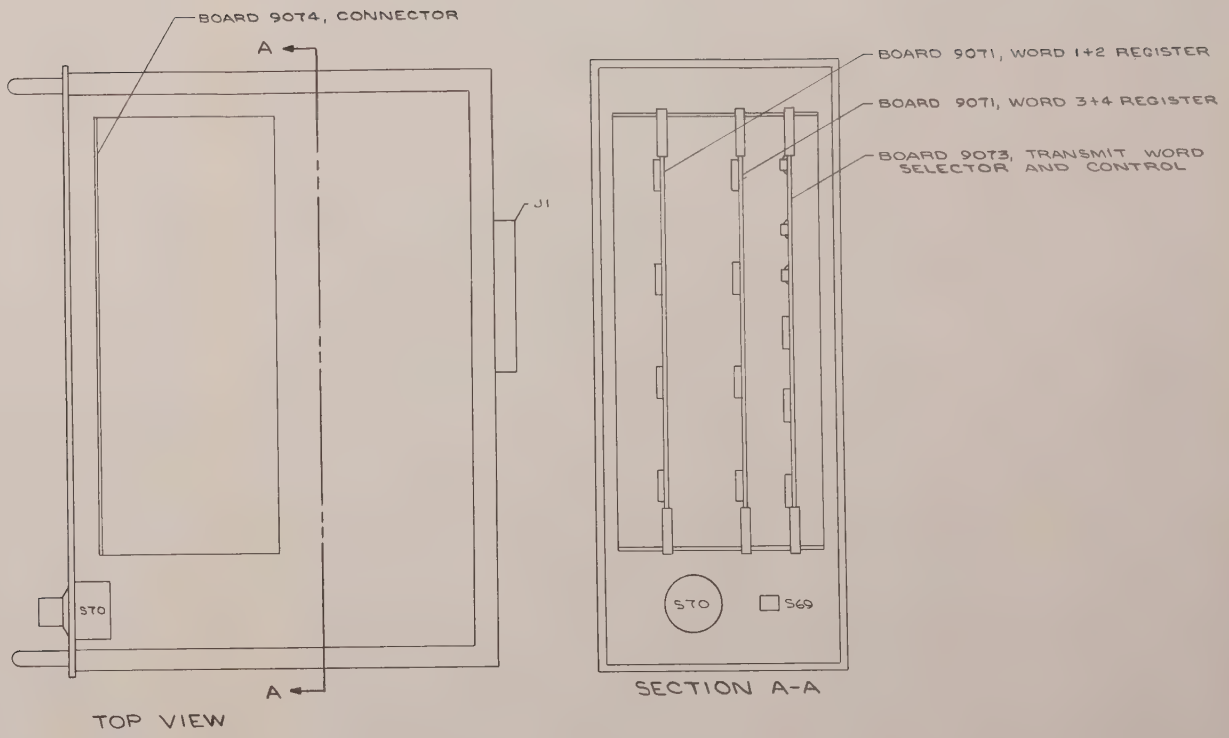


FIGURE 7-32
TRANSMIT WORD SELECTOR
MODEL 2475



REPLACEABLE PARTS LIST

SYMBOL	DESCRIPTION
J1	Connector, Amphenol No.26-4401-32P
R1-R4	Resistor, 10K, ±10%, 1/4W, A-B Type CB
S69	Switch, Toggle, SPDT, C&K No.7101-SYCB
S70	Switch, Rotary, Quan-Tech No.5198-5

FIGURE 7-33
COMPONENT AND PRINTED CIRCUIT BOARD LOCATIONS
MODEL 2477

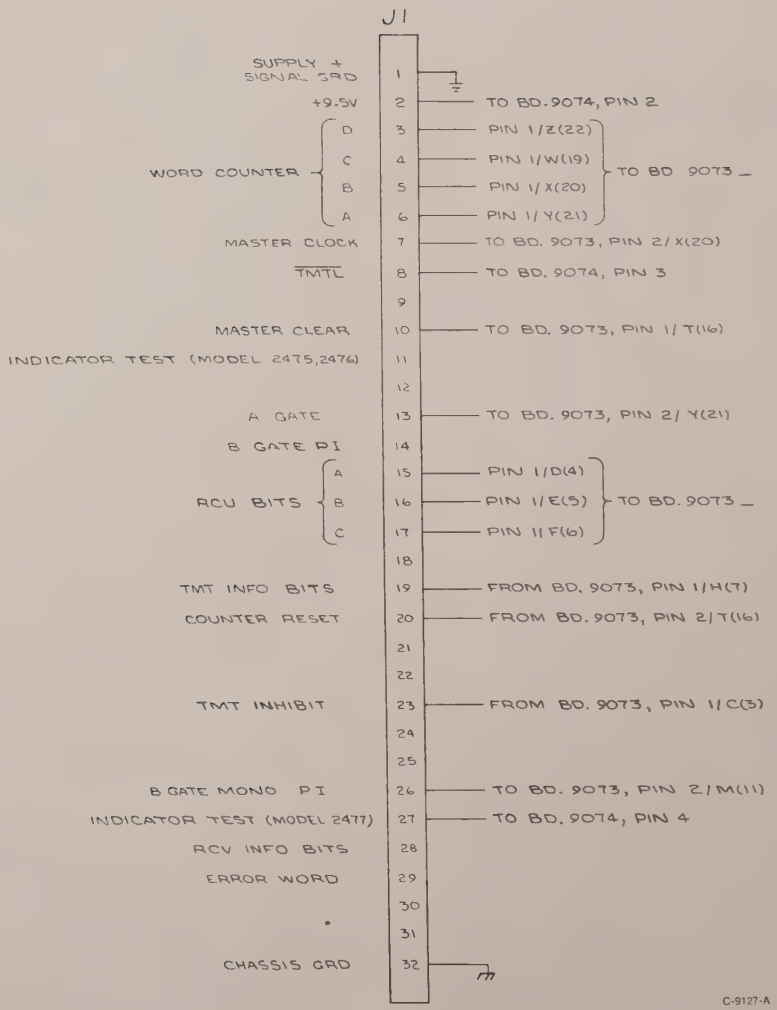
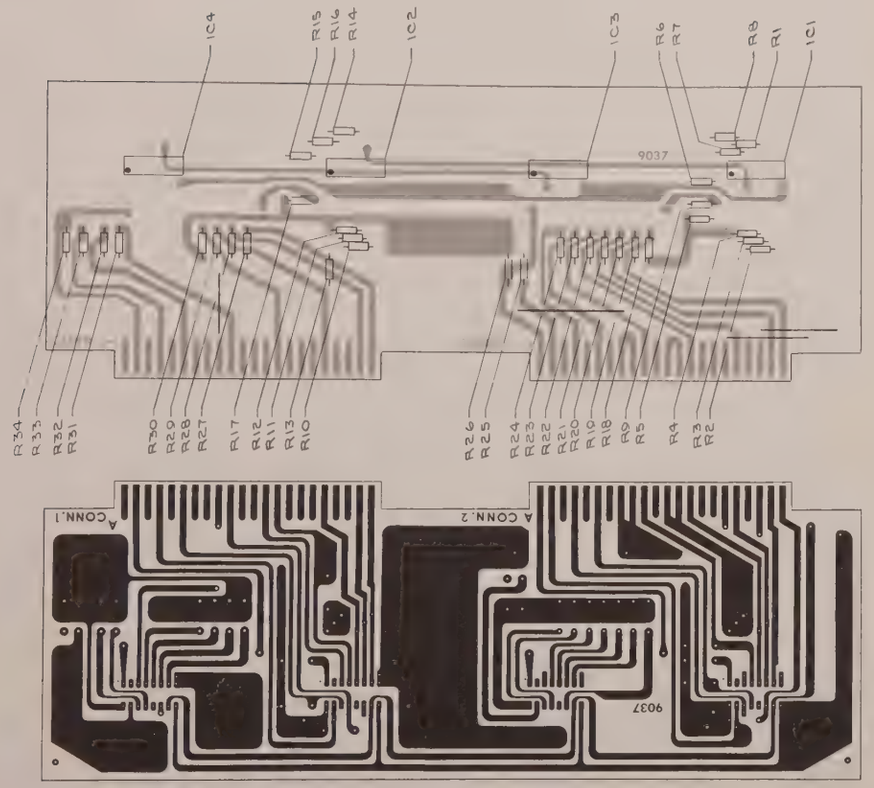


FIGURE 7-34
SCHEMATIC
CONNECTOR (PI TO BTS)
MODEL 2477

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9071 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9037 Ejector, SAE No.6100 (2 Req'd)
IC1-IC4	Integrated Circuit, CD4021AE
R1-R34	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB



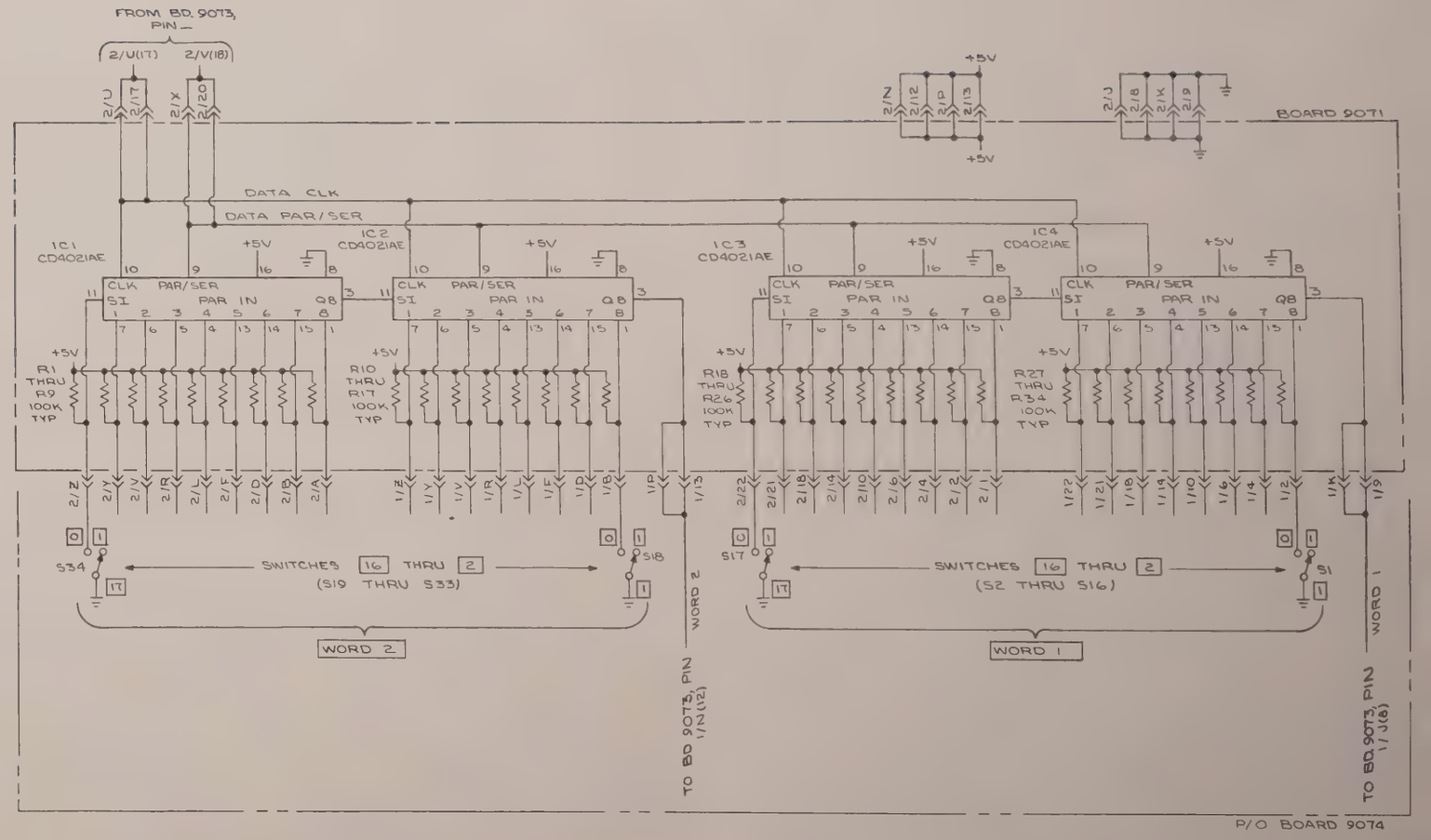


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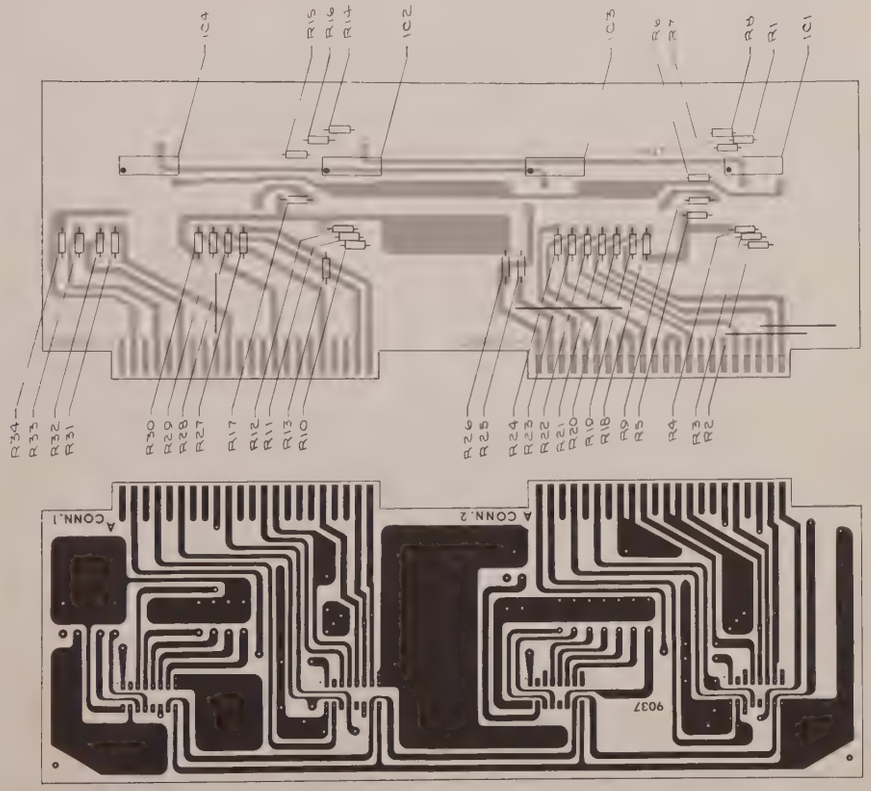
FIGURE 7-35
WORD 1 & 2 REGISTER
MODEL 2477

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9071 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9037 Ejector, SAE No.6100 (2 Req'd)
IC1-IC4	Integrated Circuit, CD4021AE
R1-R34	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB



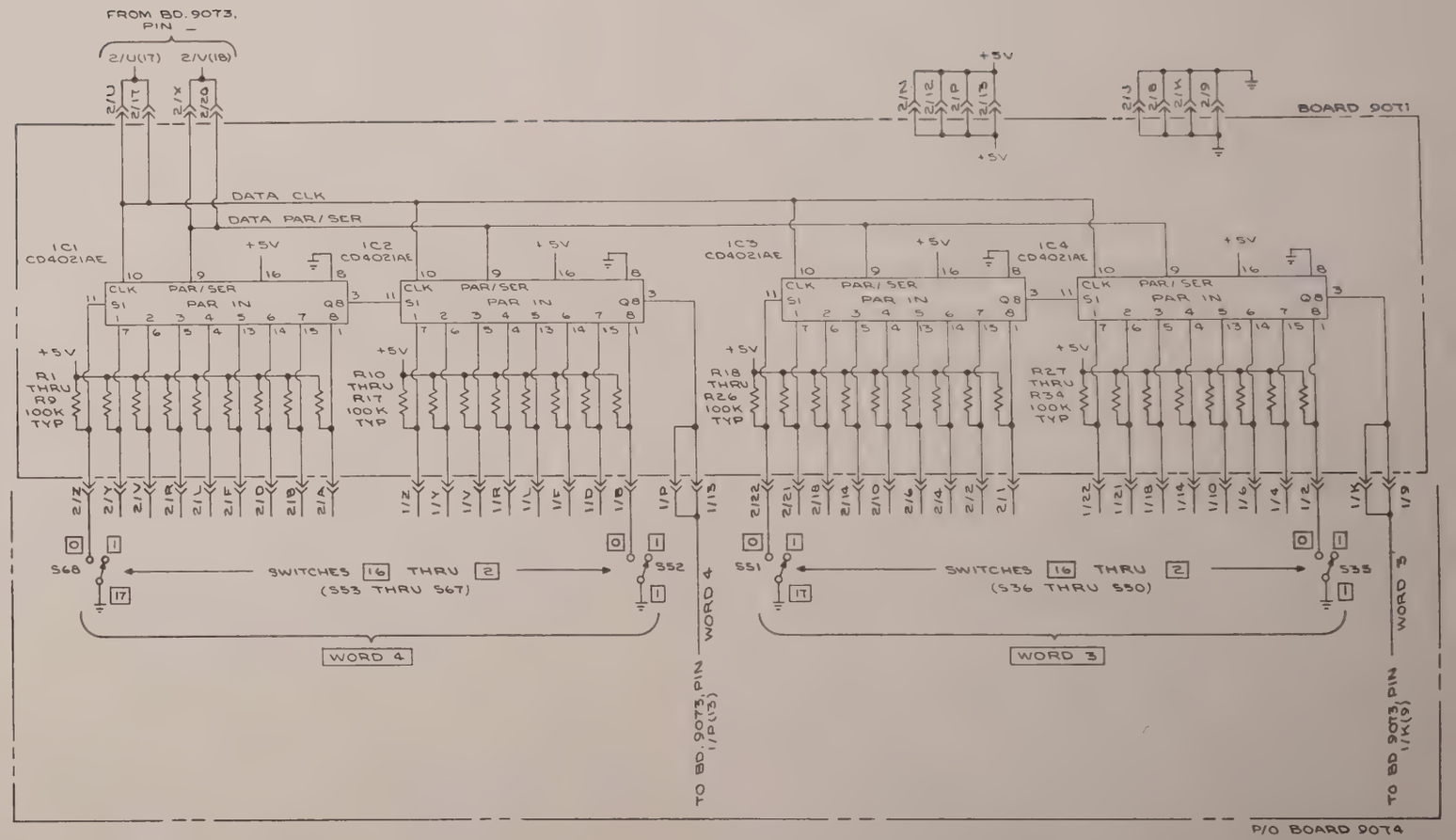
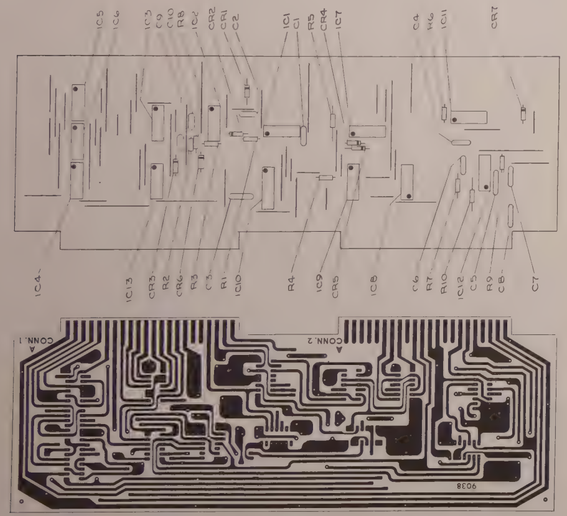


FIGURE 7-36
WORD 3 &4 REGISTER
MODEL 2477

REPLACEABLE PARTS LIST

QUAN-TECH ASSY. 9073 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9038
	Ejector, SAE No.6100 (2 Req'd)
C1,C2	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C3	Capacitor, 0.01 mF, ±20%, 1000V, Erie Type 811
C4,C5	Capacitor, 470 pF, ±10%, 1000V, Centralab No.DD-471
C6	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
C7	Capacitor, 4700 pF, ±20%, 1000V, Centralab No. DD-472
C8	Capacitor, 47 pF, ±10%, 1000V, Centralab No.DD-470
C9,C10	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No.5GA
CR1-CR7	Diode, 1N9148
IC1	Integrated Circuit, CD4002AE
IC2,IC3	Integrated Circuit, CD4013AE
IC4	Integrated Circuit, CD4023AE
IC5	Integrated Circuit, CD4011AE
IC6	Integrated Circuit, CD4001AE
IC7,IC8	Integrated Circuit, CD4011AE
IC9	Integrated Circuit, CD4012AE
IC10	Integrated Circuit, 74L85N
IC11	Integrated Circuit, CD4011AE
IC12	Integrated Circuit, CD4013AE
IC13	Integrated Circuit, CD4016AE
R1	Resistor, 22K Ohms, ±10%, 1/4W, A-B Type CB
R2	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R3,R4	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R5	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R6	Resistor, 33K Ohms, ±10%, 1/4W, A-B Type CB
R7,R8	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB
R9	Resistor, 15K Ohms, ±10%, 1/4W, A-B Type CB
R10	Resistor, 100K Ohms, ±10%, 1/4W, A-B Type CB


C5 C3 IC7 C2 R8 C7 CR2 CR1 C2
IC1 R5 CR4 IC7
C4 IC6 IC1 CR7
IC4 IC13 CR5 R2 CR6 R3 C5 R1 IC10 R4 IC9 CR3 IC8 C6 R7 R10 IC12 C1 R9 C8 C7
CONN. 1
CONN. 2
9038

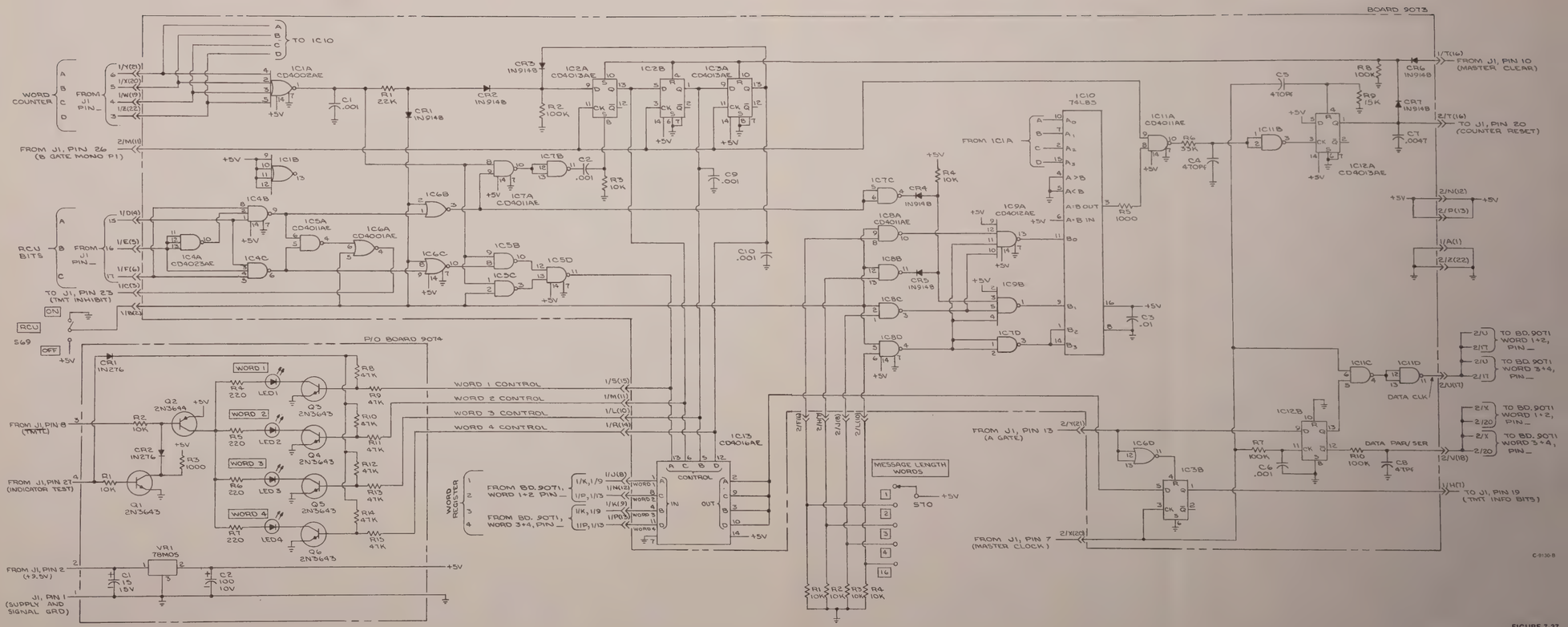
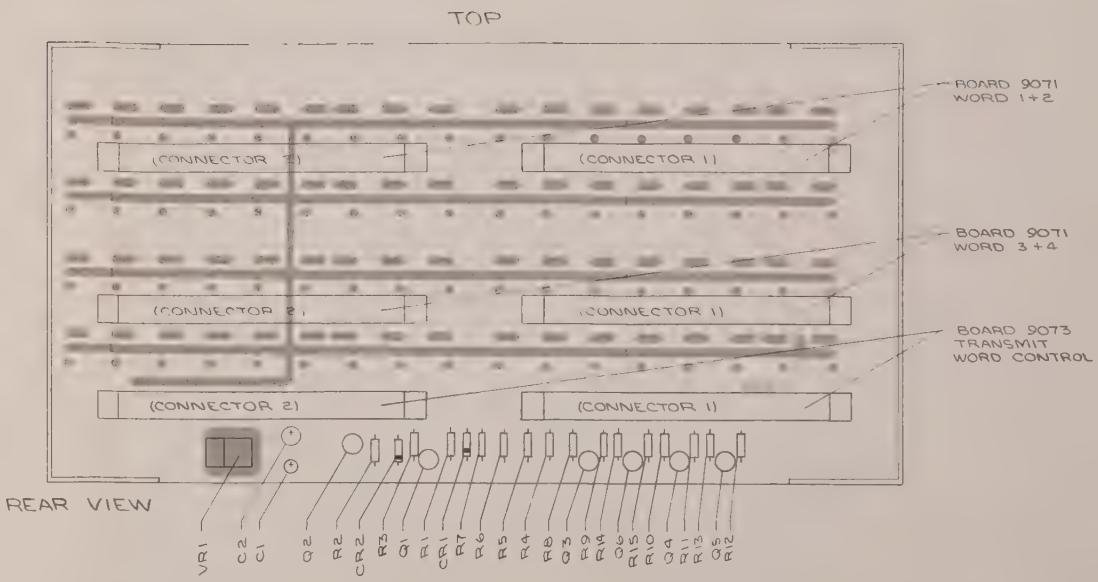


FIGURE 7-37
TRANSMIT WORD SELECTOR AND CONTROL
MODEL 2477

REPLACEABLE PARTS LIST
QUAN-TECH ASSY. 9074 CONSISTING OF:

SYMBOL	DESCRIPTION
	Board, P. C., Quan-Tech No.9039 Connector, Cinch Jones No.250-22-30-170 (2 Req'd) Connector, Cinch Jones No.252-22-30-160 (4 Req'd)
C1	Capacitor, 15 mF, ±10%, 15V, Sprague Type 196D
C2	Capacitor, 100 mF, ±20%, 10V, Sprague Type 196D
CR1,CR2	Diode, 1N276
LED1-LED4	Indicator, Monsanto No.MV-5054-3
Q1	Transistor, 2N3643
Q2	Transistor, 2N3644
Q3-Q6	Transistor, 2N3643
R1,R2	Resistor, 10K Ohms, ±10%, 1/4W, A-B Type CB
R3	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
R4-R7	Resistor, 220 Ohms, ±10%, 1/4W, A-B Type CB
R8-R15	Resistor, 47K Ohms, ±10%, 1/4W, A-B Type CB
S1-S68	Switch, Toggle, C&K No.7101-SYCB
VR1	Voltage Regulator, Fairchild No.78M05



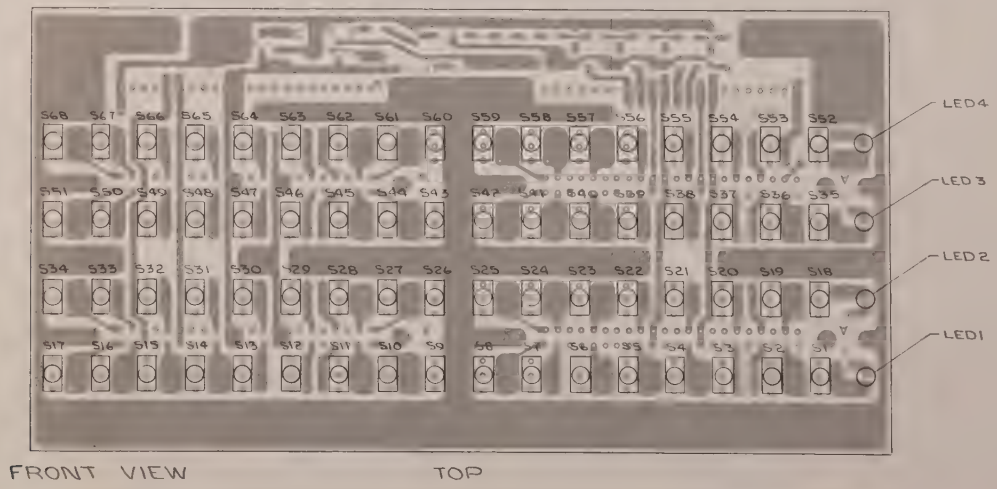
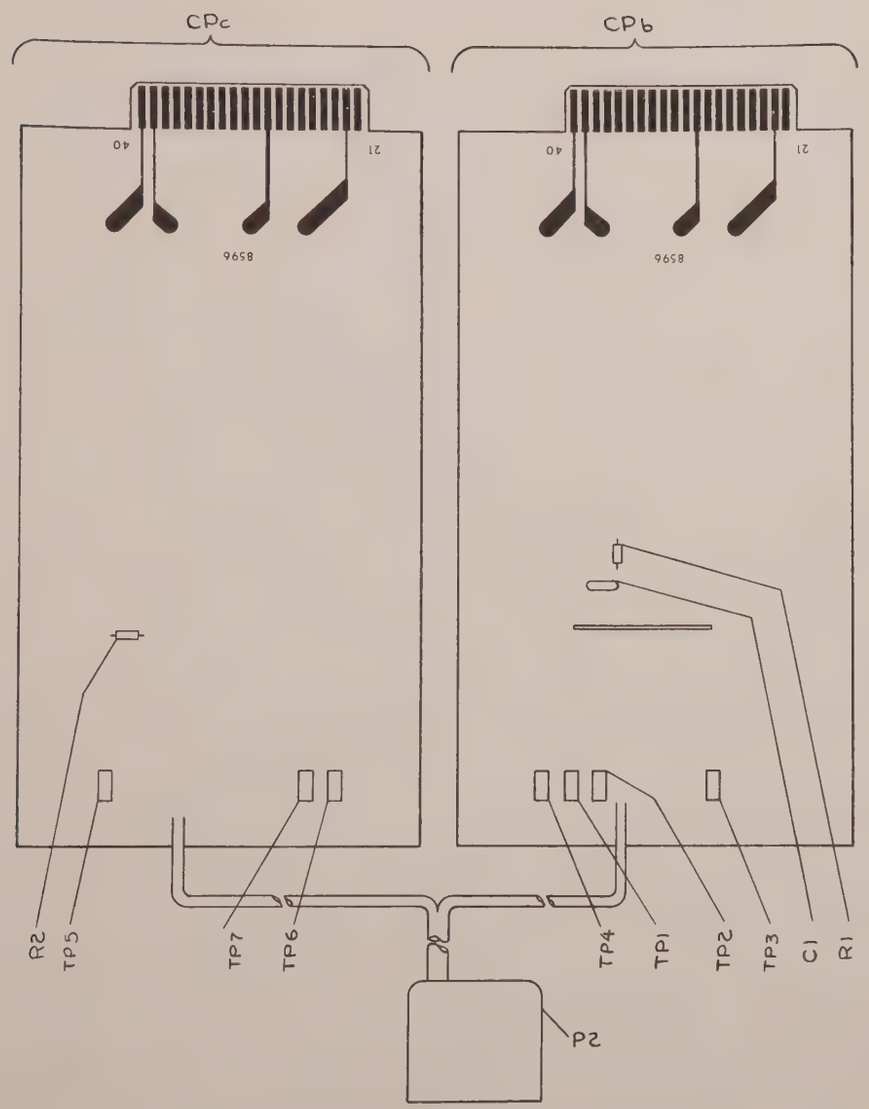
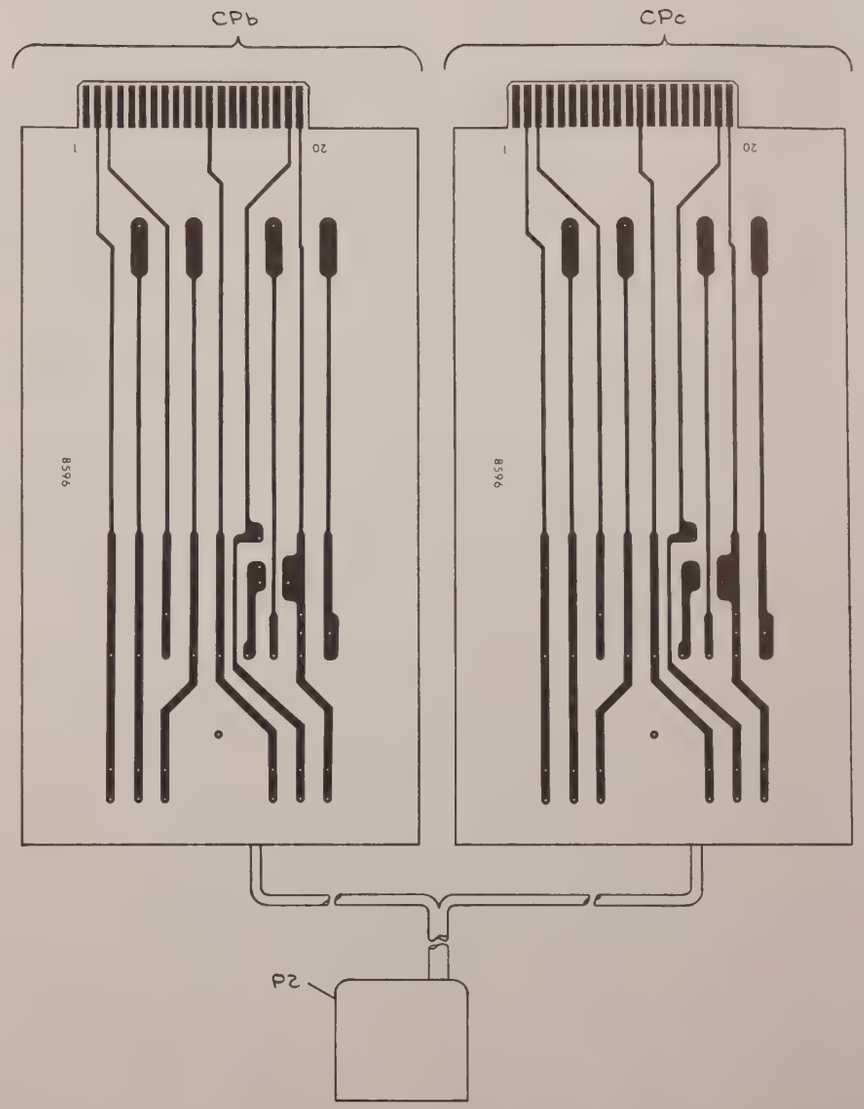


FIGURE 7-38
CONNECTOR
MODEL 2477





REPLACEABLE PARTS LIST

QUAN-TECH No.8592, E1/E2 TEST CABLE, CONSISTING OF:

SYMBOL	DESCRIPTION
P2	Connector, Amphenol No.26-4301-16S
CPb	Test Circuit Pack 1-1/D
CPc	Test Circuit Pack 1-1/B

NOTE: TEST CIRCUIT PACK 1-1/D CONSISTS OF:

C1	Capacitor, 0.001 mF, ±20%, 1000V, Sprague No 5GA
R1	Resistor, 18K Ohms, ±10%, 1/4W, A-B Type CB
TP1-TP4	Test Point, E. F. Johnson No.105-0752-02
	Card Extender, Quan-Tech No.8596-1

NOTE: TEST CIRCUIT PACK 1-1/B CONSISTS OF:

R2	Resistor, 1K Ohms, ±10%, 1/4W, A-B Type CB
TP5-TP7	Test Point, E. F. Johnson No.105-0752-02
	Card Extender, Quan-Tech No.8596-2

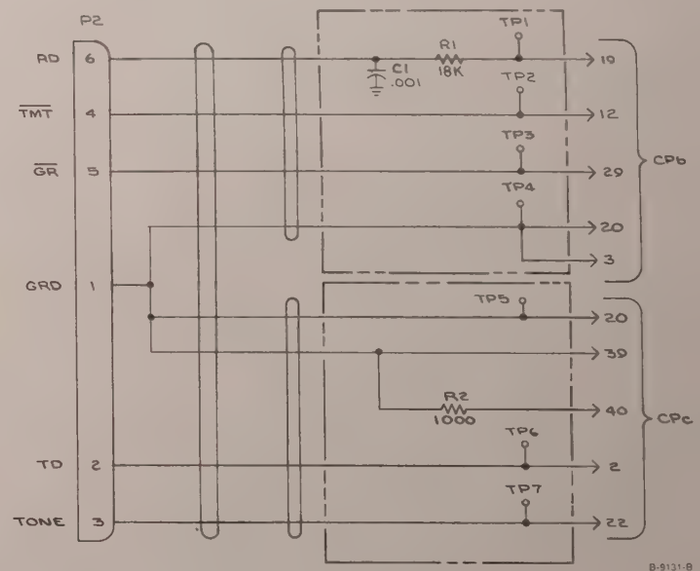
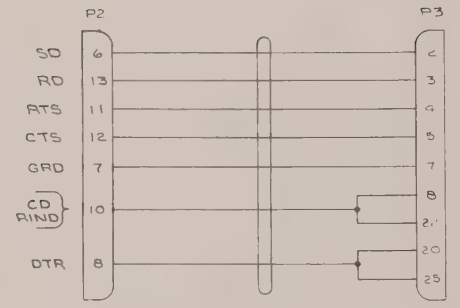


FIGURE 7-39
E1/E2 TEST CABLE
8592



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REPLACEABLE PARTS LIST
QUAN-TECH No.8593, E2A TEST CABLE, CONSISTING OF:

SYMBOL	DESCRIPTION
P2	Connector, Amphenol No.26-4301-16S
P3	Connector, Cinch No.DB-25S-C7 With No.DB-19977-2 Hood

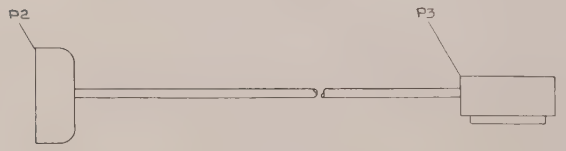
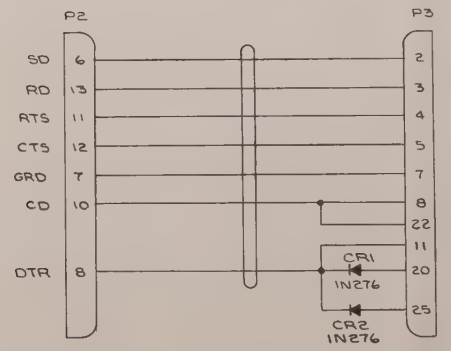


FIGURE 7-40
E2A TEST CABLE
8593



A-9133-B

REPLACEABLE PARTS LIST
QUAN-TECH No.8597, TCT TEST CABLE, CONSISTING OF:

SYMBOL	DESCRIPTION
CR1,CR2	Diode, 1N276
P2	Connector, Amphenol No.26-4301-16S
P3	Connector, Cinch No.DB-25P-C7 With No.DB-51226-1 Hood

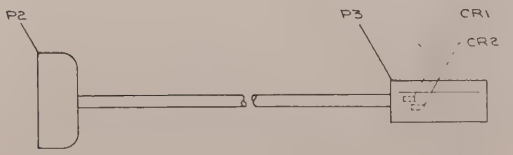
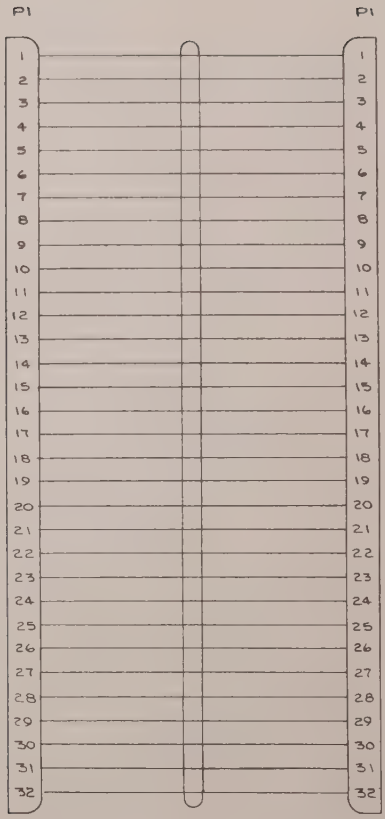
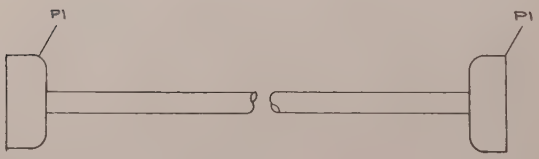


FIGURE 7-41
TCT TEST CABLE
8597



B-9135-A



REPLACEABLE PARTS LIST

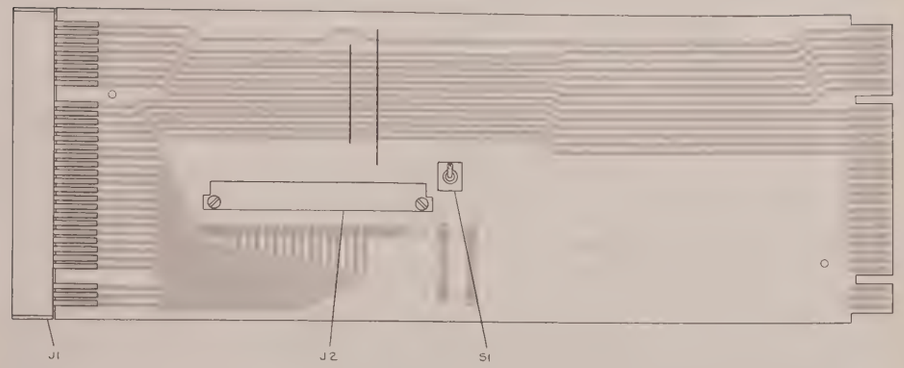
QUAN-TECH No.8770, CABLE (BTS TO P1), CONSISTING OF:

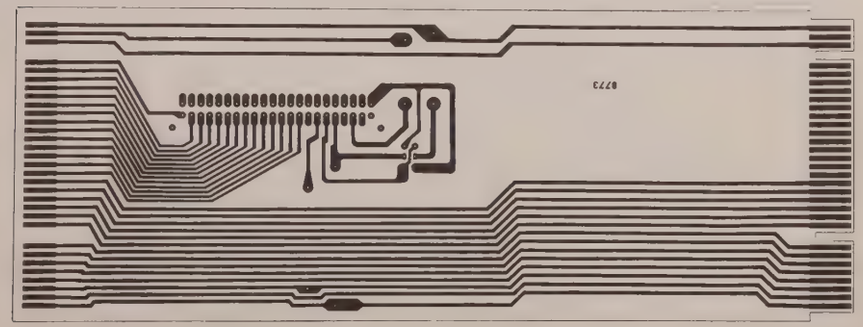
SYMBOL	DESCRIPTION
P1	Connector, Amphenol No.26-4501-32S (2 Req'd)

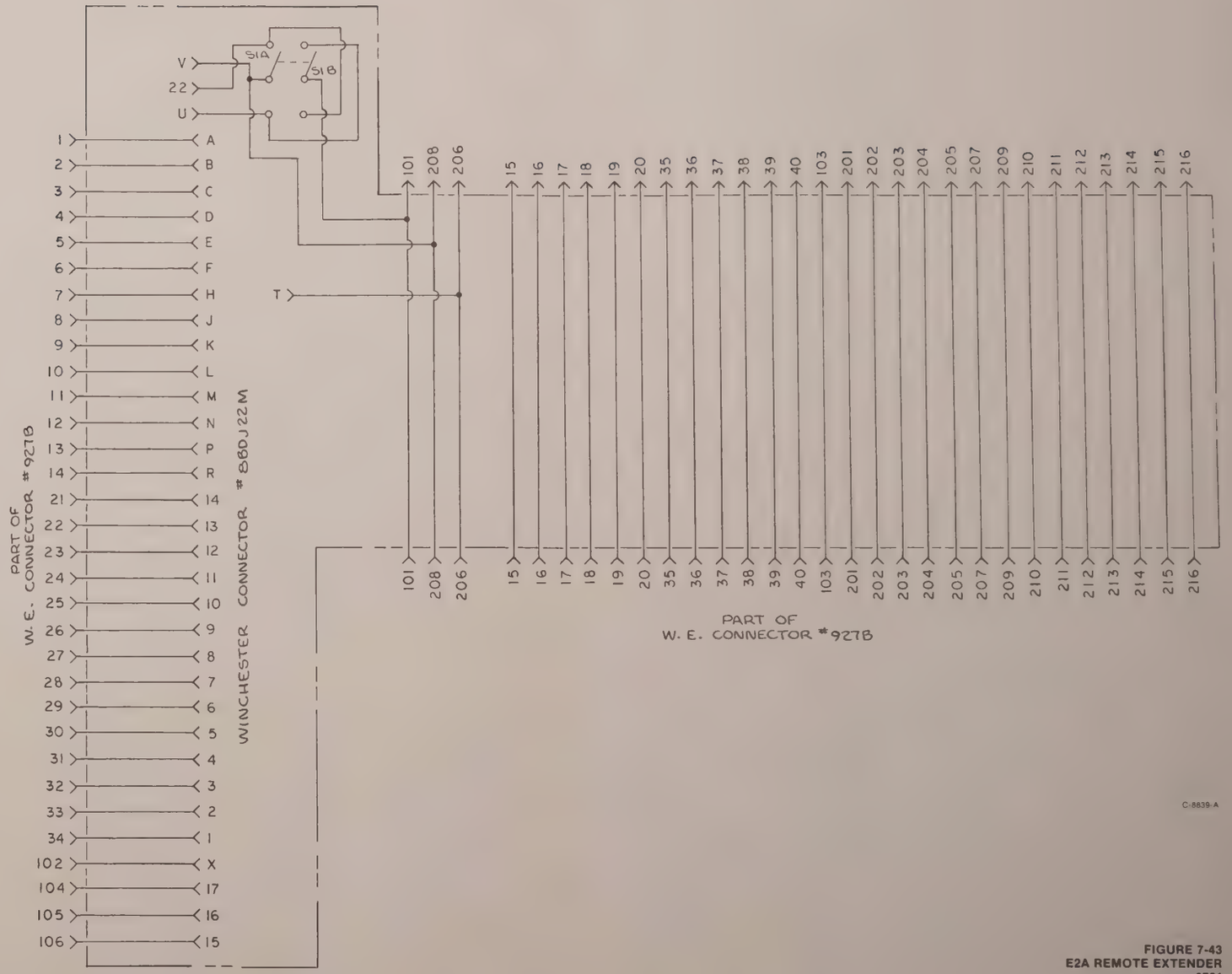
FIGURE 7-42
INTERCONNECTING CABLE (BTS TO P1)
8770

REPLACEABLE PARTS LIST
QUAN-TECH No. 8721, REMOTE TEST EXTENDER

SYMBOL	DESCRIPTION
S1	Switch, C&K No. 7201 SYCB
J2	Connector, Winchester No
J1	Connector, Western Electric No. 927B
	Board, P.C., Quan-Tech No. 8773-2





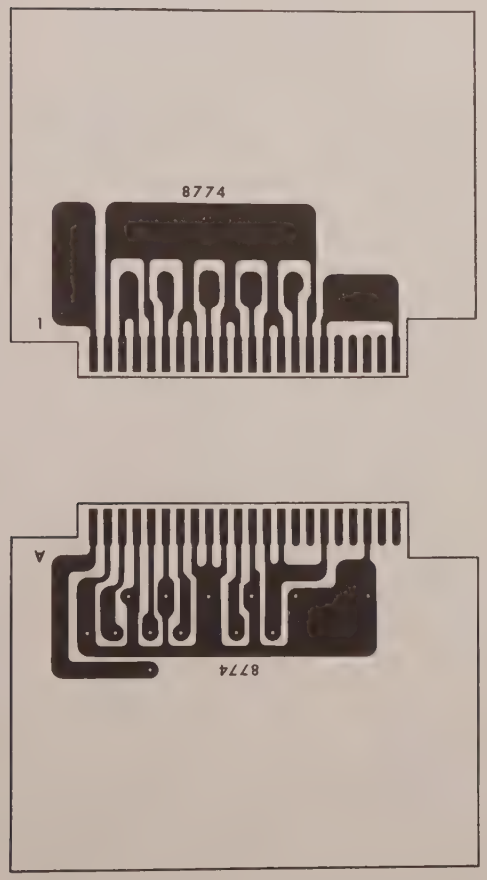


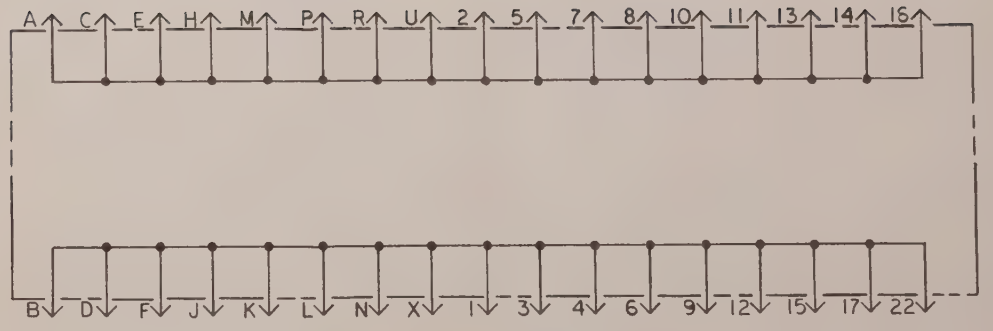
C-8839-A

FIGURE 7-43
E2A REMOTE EXTENDER
8721

REPLACEABLE PARTS LIST
QUAN-TECH No. 8722 STATUS SCANNER TESTER

SYMBOL	DESCRIPTION
	Board, P.C., Quan-Tech No. 8774-2



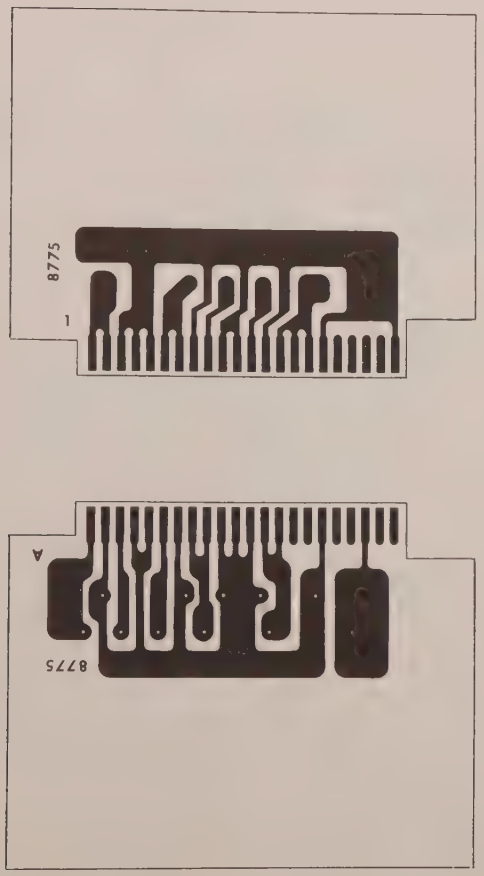


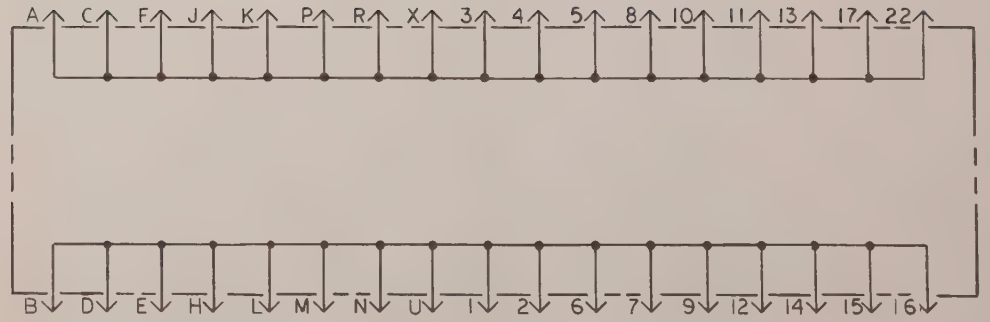
B-8840-A

FIGURE 7-44
E2A SS TESTER
8722

REPLACEABLE PARTS LIST
QUAN-TECH No. 8723 PAIRER STATUS SCANNER

SYMBOL	DESCRIPTION
	Board, P.C., Quan-Tech No. 8775-2



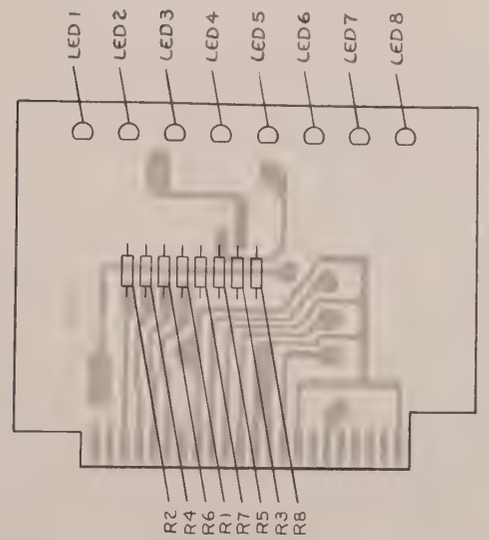


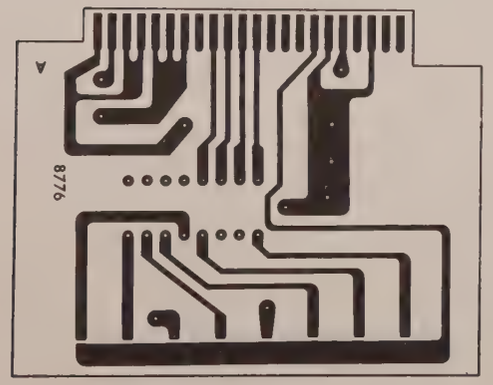
B-8841-A

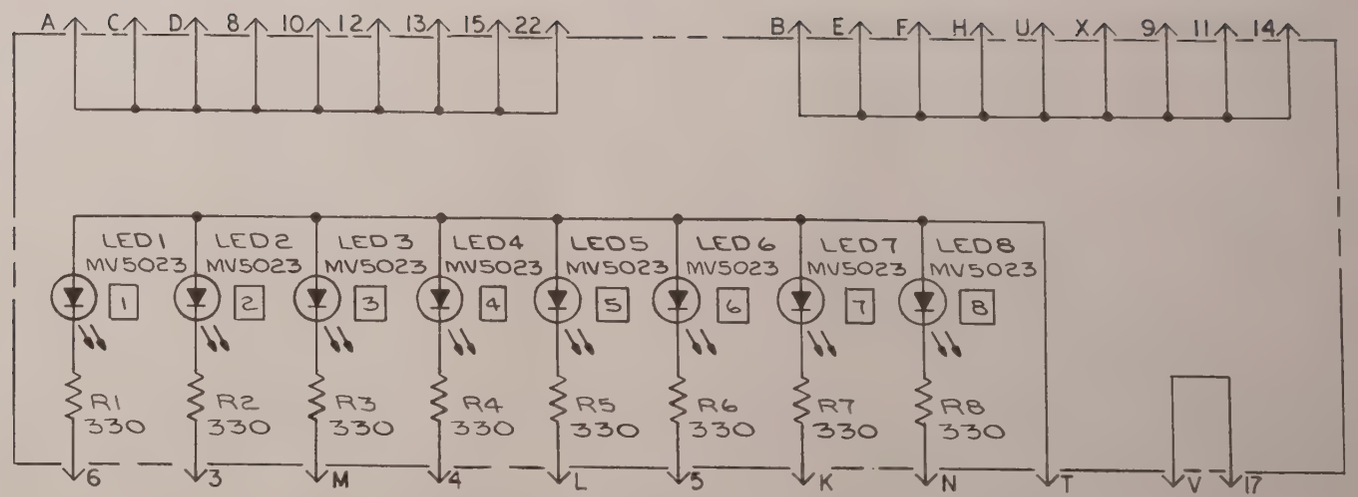
FIGURE 7-45
E2A PS TESTER
8723

REPLACEABLE PARTS LIST
QUAN-TECH No. 8724 COMBINED I/O TESTER

SYMBOL	DESCRIPTION
LED 1 – LED 2	Lamp, Monsanto MV 5023
R1 – R8	30 ohms, ±10%, ¼W, AB Type CB
	Board, P.C., Quan-Tech No. 8776-2





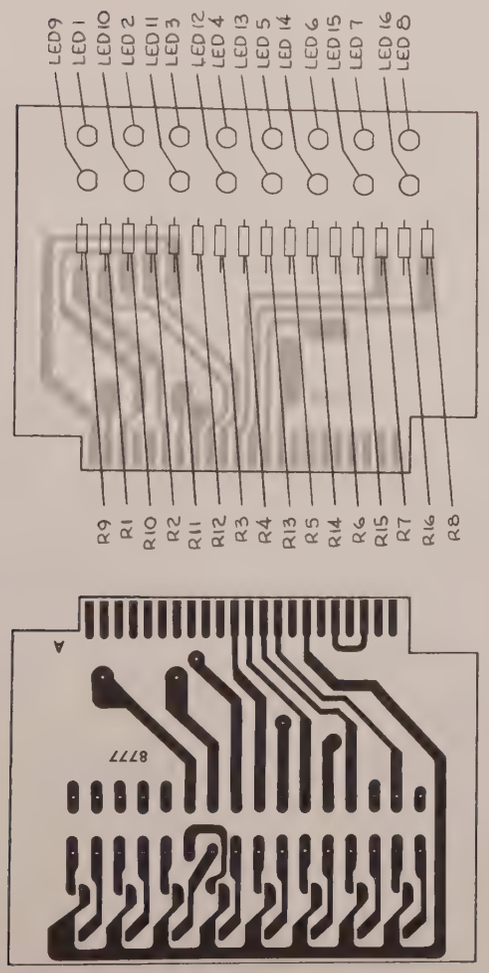


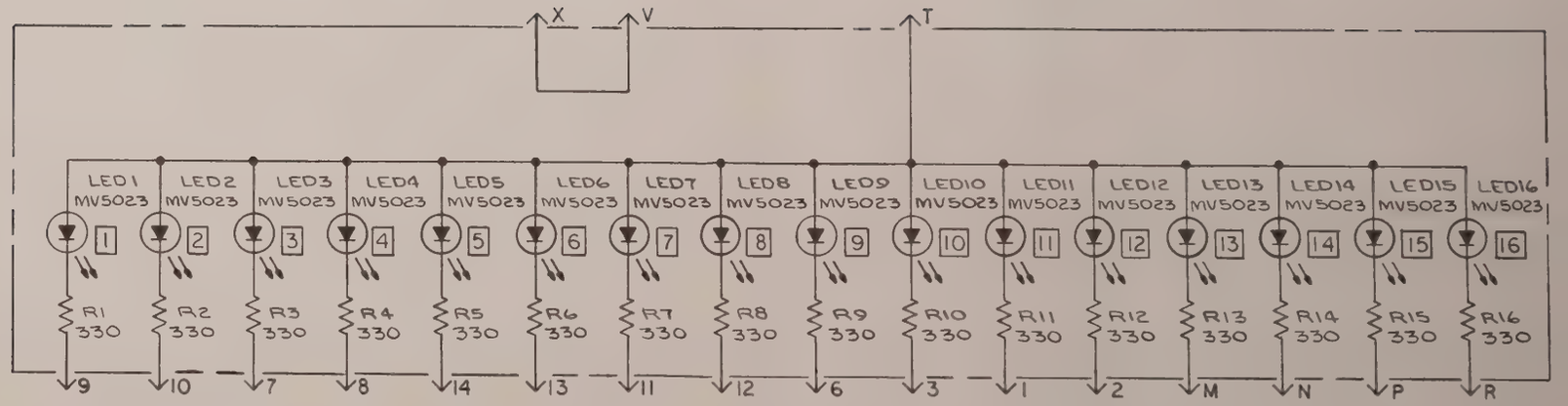
B-8842-A

FIGURE 7-46
E2A C1/O TESTER
8724

REPLACEABLE PARTS LIST
QUAN-TECH No. 8725 COMMAND DECODER TESTER

SYMBOL	DESCRIPTION
LED 1 – LED 16	Lamp, Monsanto No. 5023
R1 – R16	Resistor, 330 ohms, ±10%, ¼W, AB Type CB
	Board, P.C., Quan-Tech No. 8777-2





B-8843-A

FIGURE 7-47
E2A CD TESTER
8725

Section 8

Manual Corrections & Engineering Changes

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